
commodore
V364

264 Hardware Specification

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REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	1	ADVANCED ENGINEERING RELEASE		
	2	PILOT PRODUCTION RELEASE	12/1/83	WLM 8FK
	A	PRODUCTION RELEASE		

UNLESS OTHERWISE SPECIFIED
TOLERANCES ON:
DECIMALS
.X ± .XX ± .XXX ± ∠'S ±

MATERIAL:

FINISH:

DRAWN BY: SJC	DATE 12-1-83	
CHKD:		
ENGR: MH	5 DEC 83	
APPR: WLM	5 DEC 83	

USED ON	NEXT ASSY
TED 264	

commodore

HARDWARE SPECIFICATION
TED 264

SIZE		RE
A	310194	A
SCALE —	SHEET 1 OF	

I. SCOPE

This document contains information concerning the architecture, hardware description, timing analysis, peripheral specification and driving software description for the Commodore system based on the 7360 I.C. (hereafter referred to as the TED I.C.) and the TED system. This document does not attempt to fully describe software aspects of the TED system and information concerning this subject can be found in the appropriate documents listed in section II.

II. RELATED DO JMENTS AND STANDARDS

7360 SPECIFICATION
7501 SPECIFICATION
MOS TECHNOLOGY DATA 3OOK 1982
SYNERTECH DATA BOOK 1983
TED 64 KEYBOARD STA)ARD
FCC CLASS B - PART 5 SUBPART H STANDARDS
FCC CLASS B - TV IN :RFACE STANDARDS
NTSC BROADCAST STAN ARDS
PAL BROADCAST STAND RDS

1. SYSTEM OVERVIEW

The TED system is based on the 7501 microprocessor, which is an HMOS version of the 6510, working in conjunction with the 7360 Ted video processor. System RAM consists of 64K bytes of dynamic RAM composed of eight 64k X 1 devices. System program is contained in two 16K X 8 ROMs, and in it's standard configuration, consists of Kernal and Basic version 3.5 . The current implementation of the architecture for the Ted system supports up to 128K X 8 of ROM banked in 16K sections. ROM can be completely banked out and RAM banked in for a true 64K of RAM (minus two 256 byte pages). This allows 60,671 bytes available for Basic. The ROM/RAM banking is controlled by the 7360 under software control.

Keyboard scanning is done by outputting the row data on the Data bus while addressing a particular register in Ted, which will in turn cause Ted to latch the column information. Joystick scanning is done in the same manner.

Peripherals consist of standard serial bus products, (1541 disk drive, serial printer, ect.) cassette, TTL Serial ASCII which is intended to drive an RS-232 adapter. The expansion port supports ROM cartridges and a parallel disk drive interface.

SUMMARY OF TED SYSTEM FEATURES

- 7501 (6502 comaptible) 8 bit CPU
- 7360 VLSI video, voice, DRAM controller
- 64KByte RAM
- 32KByte ROM for use in Kernal and Basic
- 32KByte ROM for Function Key software
- 32KByte ROM for Cartridge software
- Version 3.5 Basic with advanced graphics and DOS
  (compatible with C64)
- 40 X 25 display with 128 colors
- 320 X 200 graphics resolution
- 2 Voices and white noise
- 64 keys including function keys
- Screen Editor with virtual windows
- Dual speed system clock for increased processing throughput
- External power supply (same as c64)
- Low chip count, high system integration

2. SYSTEM ARCHITECTURE

The Ted system employs a shared bus concept which allows the video processor and the microprocessor to access the same memory and I/O devices on alternate halves of the system clock. Bus access control is generated by the 7360. To increase microprocessor throughput, when this interleaving is not needed, the system clock doubles in frequency and the microproccessor is allowed full time on the bus. This occurs when no video information is being fetched by the 7360 (horizontal or vertical retrace, blank screen). There is an exception to this, and that is when the 7360 DMA's the 7501 micro to accomplish attribute fetch and character pointer information.

Dynamic RAM control signals are generated by the 7360. /RAS is generated once each memory cycle, while /CAS is generated depending on whether the memory cycle is a DRAM memory cycle or not. MUX is generated to control the multiplex of the Row and Column addresses going to the DRAMs. MUX also controls the holdoff of the R/W line as generated by the 7501. The R/W line is latched by the 7501 until the MUX line goes high signifying the end of the memory cycle. Refresh is provided by the 7360, refreshing 5 row locations (RAS only refresh) every raster line.

Selection of either ROM or RAM is accomplished by writing a bit in a Ted register. When RAM is selected, the whole 64K memory map is comprised of RAM with the exception of 2 registers for 7501 port, 1 page for Ted control registers, and 1 page for I/O. This method yields 60,671 bytes of RAM available for Basic program storage. When ROM is selected, the program residing in ROM appears in place of RAM. The exception to this is a write operation to ROM will always 'bleed through' to underlying RAM.

Kernal and Basic can also be selectivly swapped out and replaced with other 16 K sections of ROM. 2 sockets are provided internally for application programs (reffered to as function key software) and address space is allocated for 2 ROMs external to the system (cartridge use, ect.). Swapping is taken care of by a Kernal routine that does not swap out, (located at $FC00).

The cassette port and the Commodore serial bus port are implimented using the zero page ports available on the 7501 and using software control of hardware handshake.

The serial bus works with Commodore serial components, except for older peripherals that have a handshake timing problem.

The User Port is intended for external RS-232 adapters, and modem adapters. Transmission and reception is accomplished using a 6551 ACIA with handshaking assistance from a 6529 single port I.C.

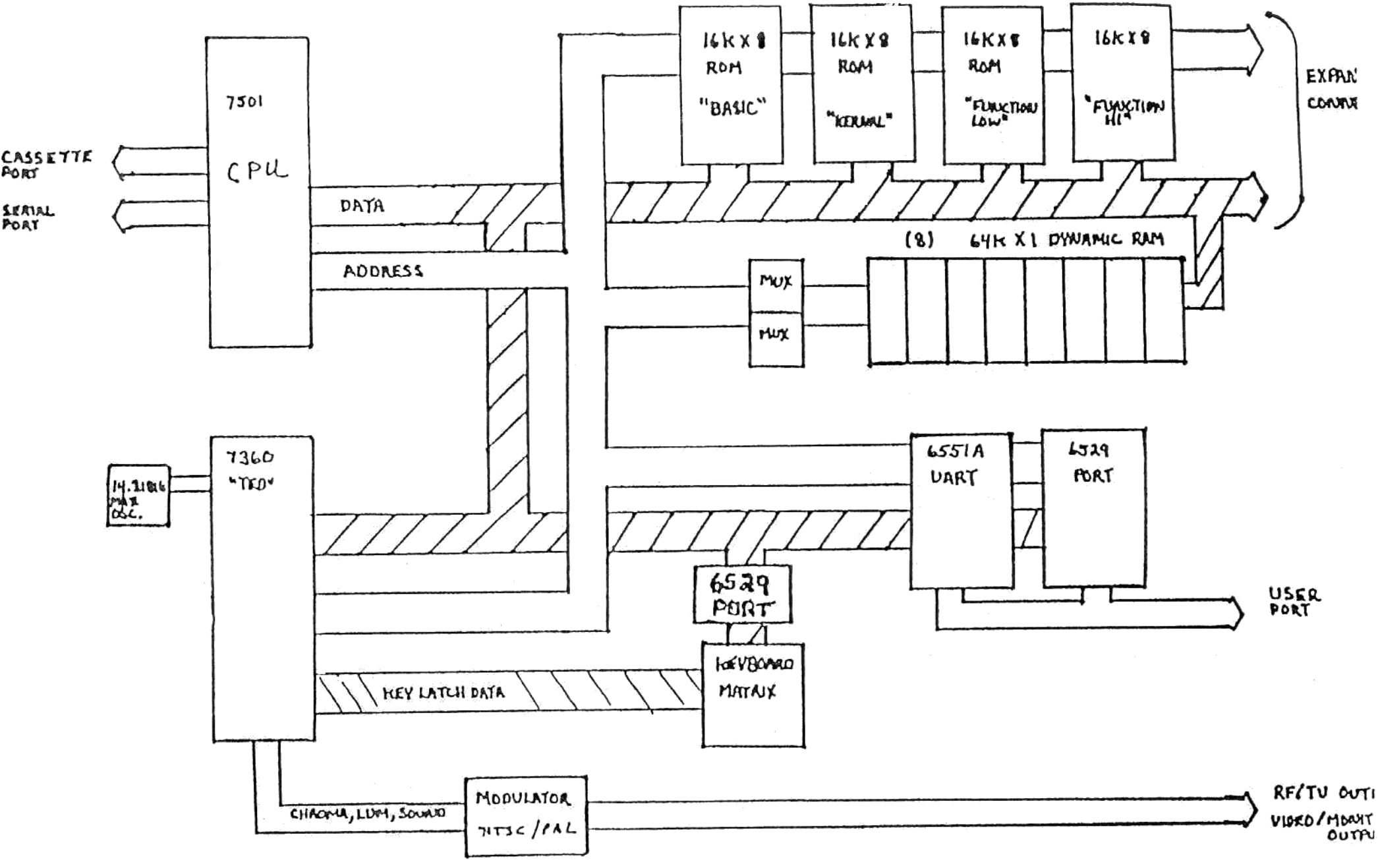
The Joystick ports are functionally compatible with the standard Commodore 5 switch type joystick. They are not compatible with analog type peripherals such as paddles, tablets, etc., as well as not being pin compatible.

The video connector has composite video as well as seperate chroma and luminance outputs for use with monitors. The 1701, 1702 type Commodore monitors interface directly to this connector.

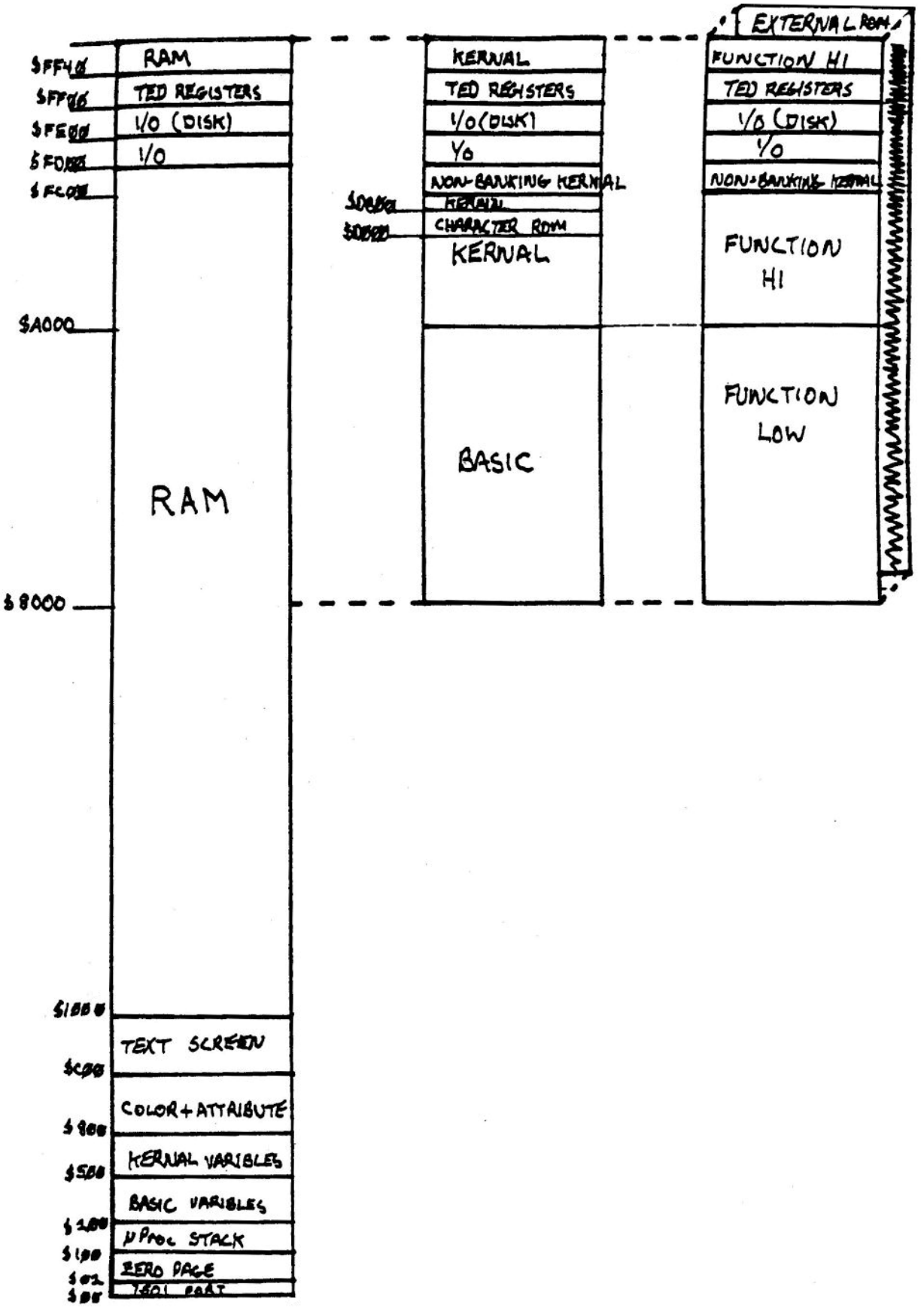
The RF output jack supplies an RF signal compatible with the regulations pertaining to TV interface devices, and is switch selectible between channels 3 and 4. Both NTSC and PAL television standards are supported.

3. SYSTEM SPECIFICATIONS

This section covers the range of system operation by discussing various constraints and features of the TED system as a whole. Included are descriptions of the system as configured and limiting factors of power, loading, and environment.



3.1 TED 64 SYSTEM DIAGRAM



3.2
TED MEMORY MAP
64K

3.3 POWER CONSUMPTION

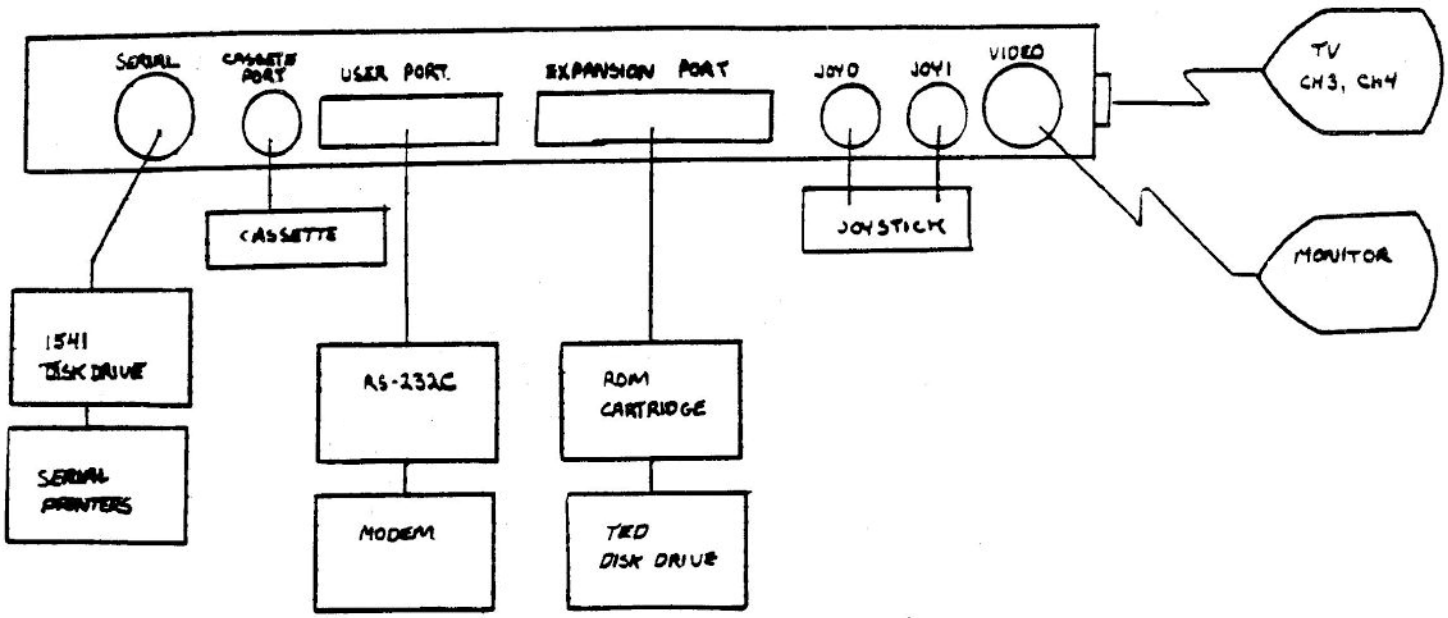
PART	I TOTAL (TYP)	I TOTAL (MAX)		
7501	80	125	ma	
7360	200	250	ma	
23128	155	220	ma	KERNAL,BASIC
74LS257	24	38	ma	
modulator	80	150	ma	
555	10	15	ma	
7406	32	51	ma	
74LS08	4	9	ma	
74LS04	4	7	ma	
7700-xx	85	120	ma	
4164-2	336	480	ma	
6551A	34	60	ma	
6529B	56	80	ma	
6529B	56	80	ma	
	1156	1685	ma	W/O FUNCTION KEY SOFTWA
23128	155	220	ma	FUNCTION KEY ROM
	1311	1905	ma	TED W/FUNCTION SOFTWARE
23128	155	220	ma	CARTRIDGE ROM
	1466	2125	ma	TED64 FUNCTION AND CART
RS - 232	1536	2225	ma	TED64 FUNC. W/CART & RS-232

** 1.53 A TYP. 2.2 A MAX. **

3.4 BUS LOADING

DEVICE	ADDRESS	DATA	R/W	RAS CAS	
7501	12	15	12	-	pf
7360	10	10	10	10	pf
4164	-	20	80	80	pf
7700	8	-	-	8	pf
6551	10	10	10	-	pf
(2)6529	-	20	20	-	pf
74LS257	5	-	-	-	pf
(2)23128	16	16	-	-	pf
	61	91	132	98	pf *
	77	107	132	98	pf **
	93	123	132	98	pf ***

* TED64
** TED64 W/FUNCTION ROMS
*** TED64 W/FUNCTION & CART



3.5
TED SYSTEM CONFIGURATION

3.6 ENVIRONMENTAL SPECIFICATION

The system is rated to operate over the range from 10 degrees Celsius to 50 degrees Celsius. Additionally, it will operate over a relative humidity range from 5% to 95% non-condensing.

4. THE 7360 TEXT DISPLAY CHIP

This chapter will discuss various aspects of the 7360 TExt Display chip.

4.1 OVERVIEW

The 7360 (or TED) is intended for low end 6502 family based, personal home computer systems.s The 7360 is a 48 pin device which controls video output, (all signals nessecary to create composite video), system timing, dynamic RAM control, ROM control, and keyboard scanning. The 7360 contains 34 control registers which are accessed through the standard 6502 microprocessor data bus. The 7360 uses the MOS technology HMOS process, and is upgradable to HMOS 2.

4.2 FEATURES

HARDWARE FEATURES:

DYNAMIC RAM REFRESH

SOUND GENERATION

PROGRAMMABLE VIDEO TIME STANDARDS
(compatible with either NTSC or PAL standards)

40 COLUMN X 25 ROW CHARACTER DISPLAY

8 X 8 CHARACTER DOT MATRIX

320 X 200 PIXEL RESOLUTION

16 UNIQUE COLORS, 8 LUMINENCE LEVELS

HARDWARE FLASH

HARDWARE CURSOR

HARDWARE REVERSE VIDEO

PROGRAMMABLE CHARACTER INFORMATION SOURCE
(ROM or RAM)

DUAL SPEED CLOCK

SCREEN BLANKING FOR DMA SENSITIVE ENVIROMENTS

4.3 CHIP CHARACTERISTICS

This section discusses some of the physical characteristics of the TED chip.

4.3.1 PINOUT

PIN	DESIGNATION	DESCRIPTION
1	A2	ADDRESS BIT 2
2	A1	ADDRESS BIT 1
3	A0	ADDRESS BIT 0
4	VCC	POWER SUPPLY +5
5	CS0	LOW ROM CHIP SELECT
6	CS1	HI ROM CHIP SELECT
7	R/W	READ/WRITE LINE
8	/IRQ	INTERUPT REQUEST
9	MUX	ADDRESS MULTIPLEX CONTROL
10	/RAS	DYNAMIC RAM ROW ADDRESS STROBE
11	/CAS	DYNAMIC RAM COLUMN ADDRESS STROBE
12	0OUT	SYSTEM CLOCK
13	COLOR	CHROMA OUTPUT
14	0IN	MASTER CLOCK
15	K0	KEYBOARD LATCH 0
16	K1	KEYBOARD LATCH 1
17	K2	KEYBOARD LATCH 2
18	K3	KEYBOARD LATCH 3
19	K4	KEYBOARD LATCH 4
20	K5	KEYBOARD LATCH 5
21	K6	KEYBOARD LATCH 6
22	K7	KEYBOARD LATCH 7
23	LUM	COMPOSITE SYNCE AND LUMINENCE
24	VSS	POWER SUPPLY GROUND
25	DB0	DATA BIT 0
26	DB1	DATA BIT 1
27	DB2	DATA BIT 2
28	DB3	DATA BIT 3
29	DB4	DATA BIT 4
30	DB5	DATA BIT 5
31	DB6	DATA BIT 6
32	DB7	DATA BIT 7
33	SND	SOUND OUTPUT
34	BA	BUS AVAILABLE
35	AEC	ADDRESS ENABLE CONTROL
36	A15	ADDRESS BIT 15
37	A14	ADDRESS BIT 14
38	A13	ADDRESS BIT 13
39	A12	ADDRESS BIT 12
40	A11	ADDRESS BIT 11
41	A10	ADDRESS BIT 10
42	A9	ADDRESS BIT 9
43	A8	ADDRESS BIT 8
44	A7	ADDRESS BIT 7
45	A6	ADDRESS BIT 6
46	A5	ADDRESS BIT 5
47	A4	ADDRESS BIT 4
48	A3	ADDRESS BIT 3

4.3.2 SIGNAL DESCRIPTION

ADDRESS BUS Pins 1 thru 3 and 36 thru 48

The 16 bit address bus is bidirectional. As an input, the microprocessor can access any of the 34 TED control registers. In the output mode TED uses the addresses to fetch Video Matrix Pointers, Attribute Pointers or character cell information. For microprocessor interface TED resides in locations FF00-FF3F in memory.

DATA BUS Pins 25 thru 36

The 8 bit data bus is also bidirectional. The data bus activity can be separated into 2 categories: microprocessor interface and video data interface during the above mentioned fetches.

KEYBOARD LATCH Pins 15 thru 22

The 8 bit keyboard latch is used as the keyboard interface. Upon instruction by the microprocessor to write to the keyboard latch, the information on the keyboard pins is latched by TED and stored until it is retrieved by the microprocessor on a read keyboard instruction. The 7360 also provides active pull ups on the keyboard matrix lines.

K0 and K1 (2 of the keyboard lines) also provide testing functions.When these pins are externally driven to 10 volts, they provide specific testing features. It should be noted however, that these pins are high impedance and if subjected to high energy electromotive fields, could cause false generation of the testing functions. This can protected against through use of diodes to insure the potential on K0 and K1 never excedes VCC. K0 generates a system freeze function, and sets all horizontal flip-flops to force TED into the dynamic RAM refresh period and single clock. All flip-flops are then released to allow their manipulation by the horizontal register. K1 forces the internal clock division into the NTSC mode.

CHIP SELECTS Pins 5 and 6

TED generates ROM chip selects based on address decoding. CS0 is active during the memory block of 8000-BFFF (HEX). CS1 corresponds to C000-FFFF (HEX) in memory. The ROM area of memory can be banked out to overlay RAM, see the description of Registers 3E and 3F (HEX).

DYNAMIC RAM CONTROL Pins 9 thru 11

TED generates /RAS and /CAS for dynamic RAM access. The signal MUX is also generated to externally multiplex the RAM row and column addresses.

READ/WRITE Pin 7

R/W is an input to TED to distinguish the type of operation to be performed. TED will actively pull up the system read line during all TED fetches. The read signal is qualified with MUX. The pin is an open source output.

INTERRUPT Pin 8

The interrupt pin is an open drain output. TED contains four interrupt sources: 3 internal timers and the raster comparator.

PHI OUT Pin 12

For increased processor throughput, TED doubles the frequency of the system clock during horizontal and vertical blanking. The actual single clock boundries are:

1) Raster lines 0-204 and horizontal positions 400-344
2) Horizontal positions 304-344

PHI IN Pin 14

For use in NTSC television systems, TED requires a 14.31818 MHZ +/- 70 ppm single phase clock input. For PAL systems, the input clock must be 17.734475 MHZ +/- 70 ppm single phase.

COMPOSITE COLOR Pin 13

The color output contains all chrominance information, including the color reference burst signal and the color of all display data. The color output is open source and should be terminated with 1K ohms to ground.

COMPOSITE SYNC AND LUMINANCE Pin 23

The luminance output contains all video synchronization as well as luminance information for the video display. The pin is open drain, requiring an external pullup of 1K Ohm.

SOUND Pin 33

This pin provides the output of the 2 tone generators. The output must be integrated through an RC network and then buffered to drive an external speaker.

BUS AVAILABLE Pin 34

Bus Available indicates the state of TED with respect to video memory fetches. BA will go low during phase 1, 3 single clock cycles before TED performs any memory access and will remain low for the entire fetch.

ADDRESS ENABLE CONTROL Pin 35

During double clock mode, AEC is always high allowing the 7501 complete control of the system buses. For single clock time periods, when BA has not gone low, AEC will toggle with PHI2 out. This allows TED PHI1, time to complete its memory accesses of video dot information while the 7501 performs during PHI2. When TED needs both halves of the cycle to perform its customary PHI1 dot fetches and PHI2 attribute and pointer fetches, BA will go low. On the fourth PHI1 out, AEC will remain low until the end of the PHI2 video fetch.

4.4 ELECTRICAL SPECIFICATIONS

This section discusses some of the electrical properties and considerations of the 7360 TED chip.

4.4.1 ABSOLUTE MAXIMUM RATINGS

INPUT VOLTAGE (Vin)	-2V to +7.0 VDC
SUPPLY VOLTAGE (Vcc)	-2V to +7.0 VDC
OPERATING TEMP (Ta)	0 to 70 'C
STORAGE TEMP	-55 to 150 'C
INPUT LEAKAGE CURRENT	-1.0 uA
DYNAMIC CHARACTERISTICS	Vcc = 5.0V +/-5%
INPUT HIGH VOLTAGE (VIH)	Vss+2.4V to Vcc+1V
INPUT LOW VOLTAGE (VIL)	VSS-2V to Vss+.8V
OUTPUT HIGH VOLTAGE (VOH) (IOH=-200uA VCC=4.75VDC)	VSS+2.4V
OUTPUT LOW VOLTAGE (VOL) (IOL=-3.2ma VCC=5.25V)	VSS+.4V
MAX POWER SUPPLY CURRENT	250ma

4.4.2 VIDEO VOLTAGE SPECIFICATIONS

CHROMA OUT	1Vp-p min. w/2VOLT OFFSET OPEN SOURCE
LUM OUT	0-5V (blanking = .5V) OPEN DRAIN

4.4.3 LUMINANCE LEVELS (R7)

LEVEL	VOLTAGE	
00	2.00	V
01	2.4	V
02	2.55	V
03	2.7	V
04	2.9	V
05	3.3	V
06	3.6	V
07	4.1	V
08	4.8	V

4.4.4 COLOR PHASE ANGLES

COLOR	HUE PHASE (relative to SIN, in degrees)	
	NTSC	PAL
BLACK	--	--
WHITE	--	--
RED	70	103
CYAN	250	283
MAGENTA	20	53
GREEN	208	241
BLUE	314	347
YELLOW	134	167
ORANGE	90	129
BROWN	115	148
YLLW-GRN	162	195
PINK	50	83
BLU-GRN	232	265
LT-BLU	290	323
DK-BLU	350	23
LT-GRN	180	213

4.5 GENERAL TIMING

This section explores the various timing considerations and constraints related to the TED chip.

4.5.1 BUS TIMING

PARAMETER	SYMBOL	MIN	MAX	UNIT
TED ADDR SETUP	TADS	-	150	ns
INPUT DATA SETUP	TDSU	50	-	ns
INPUT DATA HOLD	TDH	10	-	ns
OUTPUT DATA STABLE	TDSO	160	-	ns
OUTPUT DATA HOLD	TDHO	80	120	ns
R/W STABLE PERIOD	TRWS	-	178	ns
MUX TO R/W SETUP	TMRWS	-	70	ns
MUX TO R/W HOLD	TMRWH	30	-	ns
CHIP SELECT SETUP	TCSS	-	320	ns
CHIP SELECT HOLD	TCSH	70	-	ns
ADDRESS HOLD	TAH	60	-	ns
ADDRESS IN TRISTATE	TADTH	-	135	ns

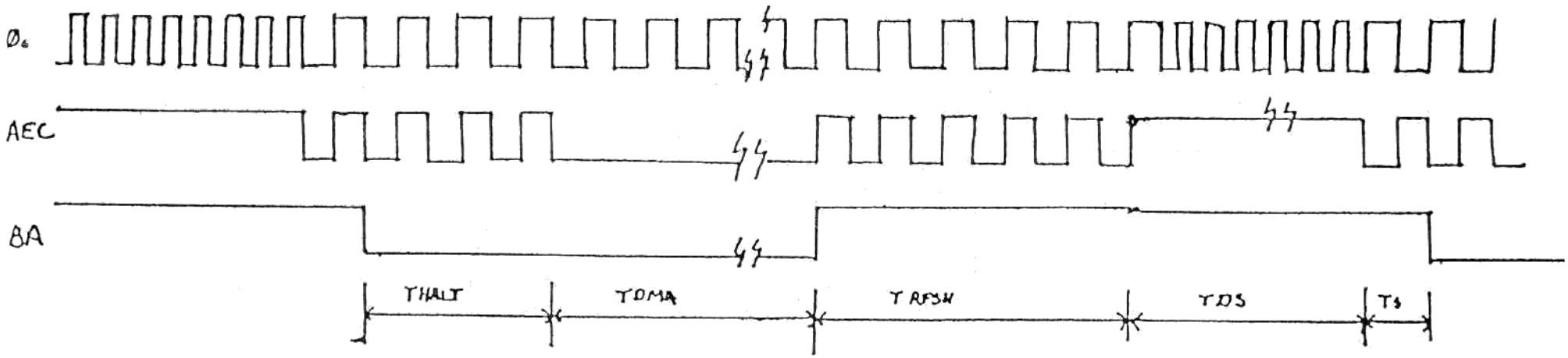
4.5.2 DMA TIMING

The 7360 performs DMA's to fetch additional information to maintain a video display. Twice per each row of characters, (a character being defined as a cell 8 X 8 bits) to obtain the attributes for each character and to obtain the character pointer which points to where the charcter pattern can be found. In bit map mode, these DMA's still occur, but the information is interpretted differently. The sequence of events in a DMA cycle are: 1)The system clock comes out of double speed for 1 cycle. At the same time AEC starts to toggle, allowing the 7360 on the bus. 2)The Bus Available line goes low. 3)Three cycles are given to the 7501 to complete operation before DMA begins. 4)40 cycles of single clock where the 7360 is doing 2 fetches per cycle. 5)BA goes high at the same time as AEC allowing the 7501 back on the bus. 6)5 cycles follow of single speed where the 7360 is engaged in refreshing the dynamic RAM. 7)16 cycles of double speed (equiv. to 8 cycles of single) 8) If last DMA was row 8 of character, then DMA for row 1 of next character is initiated. If screen is blanked, the 5 cycles of single speed are still present for dynamic RAM refresh.

4.5.2.1 TED DMA TIMING (REFER TO 4.5.2.2 TED DMA TIMING DIAGRAM)

	cycles	time	
TDMA	40	46us	TIME, DMA
THALT	3	3us	TIME, HALT
TRFSH	5	5us	TIME, REFRESH
TDS	16	9us	TIME, DOUBLE SPEED
TS	1	1us	TIME, SYNCHRONIZE

Diagram 4.5.2.2 represents the occurence of when two DMAs are 'back to back', I.E. character row 8 DMAs, then character row 1 of the next character DMAs, seperated only by one horizontal retrace.



4.5.2.2 TED DMA TIMING DIAGRAM

4.5.3 VIDEO TIMING

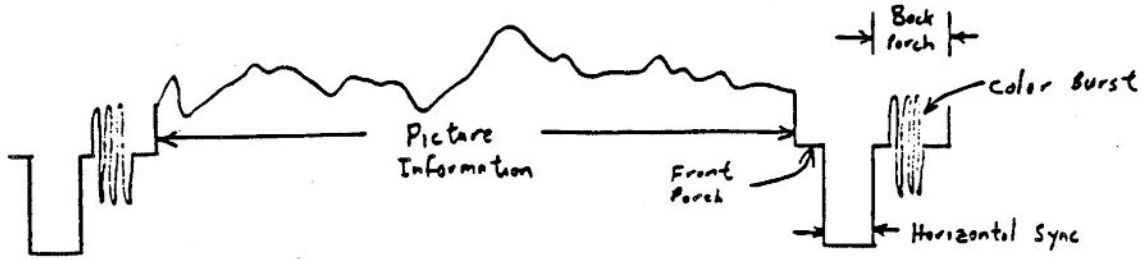
This subsection discusses some of the properties of the TED video section timing.

4.5.3.1 HORIZONTAL TIMING

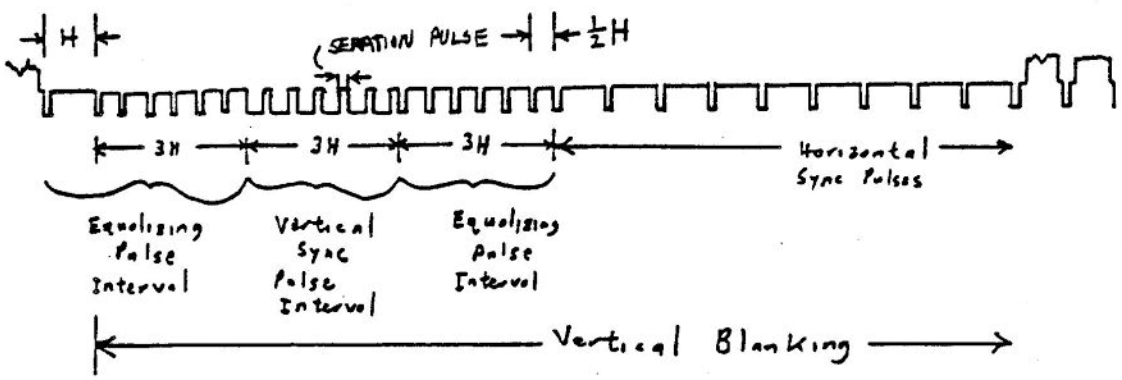
PERIOD	TIME NTSC	PAL
TOTAL LINE	63.5 uS	64 uS
H BLANKING	9.5 - 11.5	uS
H SYNC PULSE	4.75 +/- 0.5	uS
FRONT PORCH	1.27 (MIN)	uS
BACK PORCH	3.81 (MIN)	uS
COLOR BURST	8-11 CYCLES 3.58MHZ +/- 250 HZ	
VISIBLE LINE TIME	52-54	uS

4.5.3.2 VERTICAL TIMING

PERIOD	TIME NTSC	PAL
TOTAL FIELD	.0167	SEC
V BLANKING	.0008-.0013	SEC
V SYNC PULSE	31.75	uS
6 V SYNC PULSES	190.5	uS
EQ PULSE	2.54	uS
SERATION PULSE	2.54	uS
VISIBLE FIELD	.015-.016	SEC



HORZ LINE



VERT LINE

4.5.3.3 VIDEO TIMING DIAGRAM

5. THE 7501 MICROPROCESSOR

This section describes some of the properties and functions of the type 7501 microprocessor.

5.1 7501 DESCRIPTION

The 7501 is an HMOS version of the 6502 family or more specifically, the 6510CBM. The 7501 is software compatible with existing 6502, 6510 code.
The 7501 contains a 7 bit bi-directional port used to directly drive the serial bus and cassette. The port is at location $0000 while the data direction register is at $0001. The 7501 is Tri-statable and through use of the AEC (address enable control) line and is used extensivly in the TED shared bus concept. DMA is accomplished using the AEC line and the RDY line (called BA on TED). A control line is provided (GATE IN) to hold off the R/W line until /RAS makes the transistion from low to hi. This prevents the Read line from making an early transistion to the write state which would cause an improper Early Write Cycle to occur.

5.2 7501 PINOUT

PIN	NAME	DESCRIPTION
1	PHI IN	SYSTEM CLOCK INPUT
2	RDY	DMA RQST
3	/IRQ	INTERUPT RQST
4	AEC	ADDRESS ENABLE CONTROL
5	VCC	POWER SUPPLY +5V.
6	A0	ADDRESS BIT 0
7	A1	ADDRESS BIT 1
8	A2	ADDRESS BIT 2
9	A3	ADDRESS BIT 3
10	A4	ADDRESS BIT 4
11	A5	ADDRESS BIT 5
12	A6	ADDRESS BIT 6
13	A7	ADDRESS BIT 7
14	A8	ADDRESS BIT 8
15	A9	ADDRESS BIT 9
16	A10	ADDRESS BIT 10
17	A11	ADDRESS BIT 11
18	A12	ADDRESS BIT 12
19	A13	ADDRESS BIT 13
20	GND	POWER SUPPLY GROUND
21	A14	ADDRESS BIT 14
22	A15	ADDRESS BIT 15
23	GATE IN	R/W GATE
24	P7	PORT BIT 7
25	P6	PORT BIT 6
26	P4	PORT BIT 4
27	P3	PORT BIT 3
28	P2	PORT BIT 2
29	P1	PORT BIT 1
30	P0	PORT BIT 0
31	DB7	DATA BIT 7
32	DB6	DATA BIT 6
33	DB5	DATA BIT 5
34	DB4	DATA BIT 4
35	DB3	DATA BIT 3
36	DB2	DATA BIT 2
37	DB1	DATA BIT 1
38	DB0	DATA BIT 0
39	R/W	READ/WRITE
40	RES	RESET

5.3 7501 ELECTRICAL SPECIFICATIONS

This section describes some of the electrical constraints and specifications of the system.

5.3.1 MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	Vcc	-0.3 to +7.0	Vdc
Input Voltage	Vin	-0.3 to +7.0	Vdc
Operating Temperature	Ta	0 to +70	C
Storage Temperature	Tstg	-55 to +150	C

5.3.2 ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	VIH				
Phi0(in)		Vss+2.4	---	Vcc	Vdc
/RES,P0-P7,/IRQ,Data		Vss+2.2	---	---	Vdc
Input Low Voltage	VIL				
Phi0(in)		Vss-0.3	---	Vss+0.5	Vdc
/RES,P0-P7,/IRQ,Data		---	---	Vss+0.8	Vdc
Input Leakage Current (Vin=0 to 5.25V, Vcc=5.25V)	Iin				
Logic		---	---	2.5	uA
Phi0(in)		---	---	10.0	uA
3-State(Off) Inp. Cur. (Vin=0.4 to 2.4V, Vcc=5.25V)	ITSI				
Data Lines		---	---	10.0	uA
Output High Voltage (IOH=-100uAdc, Vcc=4.75V)	VOH				
Data,A0-A15,R/W,P0-P7		Vss+2.4	---	---	Vdc
Output Low Voltage (IOL=1.6mAdc, Vcc=4.75V)	VOL				
Data,A0-A15,R/W,P0-P7		---	---	Vss+0.4	Vdc
Power Supply Current	ICC	---	125	---	mA
Capacitance (Vin=0,Ta=25 C, f=1MHz)	C				
Logic,P0-P7	Cin	---	---	10	pF
Data	Cout	---	---	15	pF
A0-A7	Cout	---	---	12	pF
Phi1	CPHi1	---	30	50	pF
Phi2	CPHi2	---	50	80	pf

5.4 SIGNAL DESCRIPTION

CLOCK (PHI 0) - This is the dual speed system clock and is a standard TTL level input.

ADDDRESS BUS (A0 - A15) - TTL output. Capable of driving 2 TTL loads at 130 pf.

DATA BUS (D0 - D7) - Bi-directional bus for transferring data to and from the device and the peripherals. The outputs are tri-state buffers capable of driving 2 standard TTL loads and 130pf.

RESET - This input is used to reset or start the uprocessor from a power down condition. During the time that this line is held low, writing to or from the uprocessor is inhibited. When a positive edge is detected on the input, the uprocessor will immediatly begin the reset sequence. After a system initialization time of 6 cycles, the mask interupt flag will be set and the processor will load the program counter from the contents of memory locations $FFFC and $FFFD. This is the start location for program control. After VCC reaches 4.75 volts in a power up routine, reset must be held low for at least 2 cycles. At this time the R/W line will become valid.

INTERUPT REQUEST (IRQ) - TTL input, request that the processor initiate an interrupt sequence. The processor will complete execution of the current instruction before recognizing the request. At that time, the interrupt mask in the Status Code Register will be examined. If the interrupt mask is not set, the processor will begin an interrupt sequence. The Program Counter and the Processor status register will be stored on the stack and the interrupt disable flag is set so that no other interrupts can occur. The processor will then load the program counter from the memory locations $FFFE and $FFFF.

ADDRESS ENABLE CONTROL (AEC) - The Address Bus is only valid when the AEC line is high. When low, the address bus is in a high impedance state. This allows easy DMA's for shared bus systems.

I/O PORT (P0-P4,P6,P7) - Bidirectional port used for transferring data to and from the processor directly. The Data Output Register is located at location $0001 and the Data Direction Register is located at location $0000.

R/W - TTL level output from processor to control the direction of data transfer between the processor and memory, peripherals, etc. This line is high for reading memory and low for writing. This line is latched by the Gate In line to synchronize between a DRAM memory cycle and the processor clock cycle. If AEC is low when Gate In makes a low to high transition, the R/W line will go to a high impedence until the next transition of the Gate In line and AEC is high prior to the transition.

GATE IN - TTL level input, used to gate the R/W line to prevent the R/W line from going low during a read cycle, before RAS and CAS go high (resulting in a Read/Write cycle). Normally connected to the MUX line in a system configuration to synchronize the DRAM memory cycle to the processor clock cycle.

RDY - Ready. TTL level input, used to DMA the 7501. The processor operates normally while RDY is high. When RDY makes a transition to the low state, the processor will finish the operation it is on, and any subsequent operation if it is a write cycle. On the next occurence of read cycle the processor will halt, making it possible to tri-state the processor to gain complete access to the system bus.

5.5 PROCESSOR TIMING

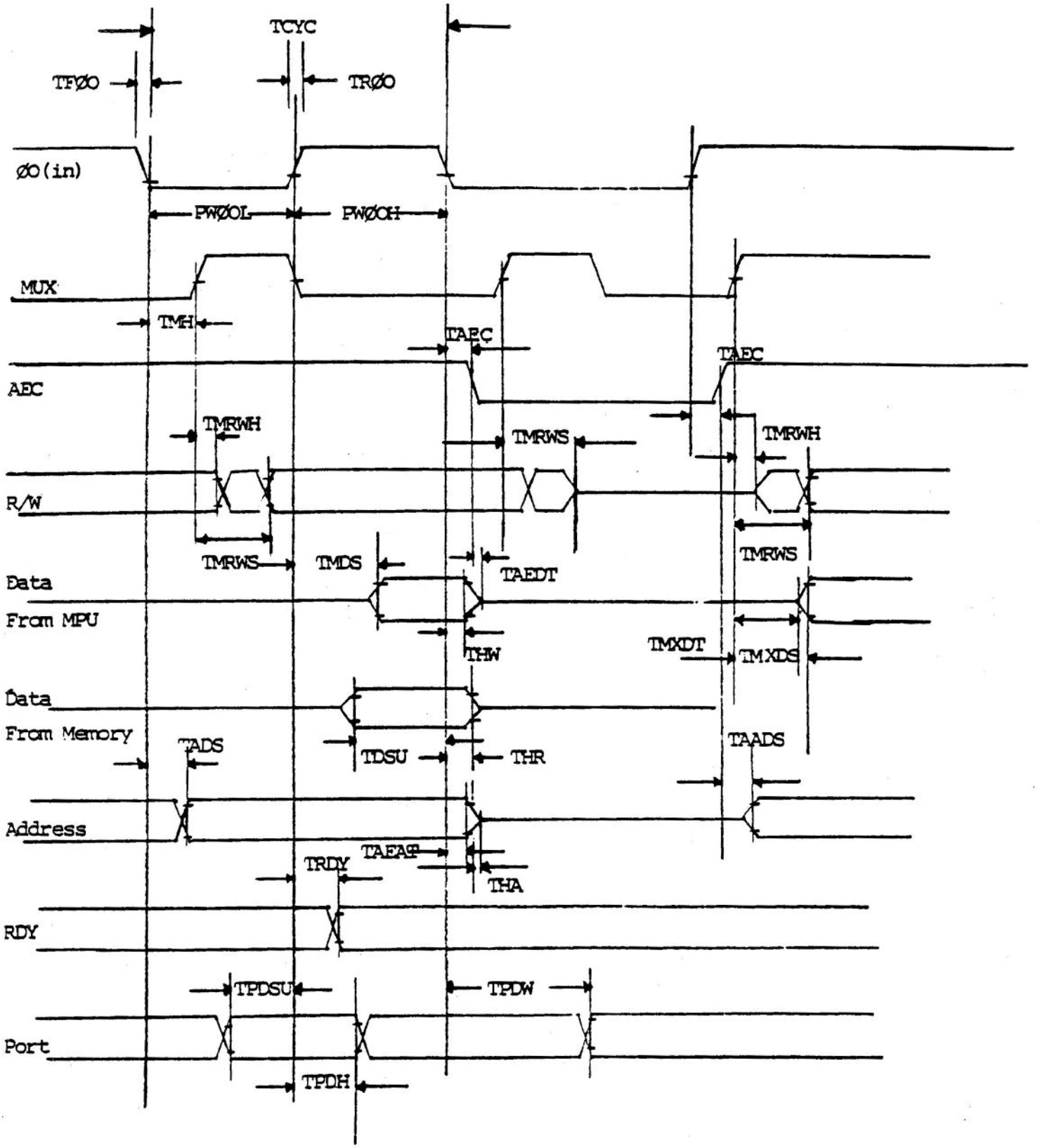
This section explores the timining considerations of the 7501 processor unit.

5.5.1 TIMING CHART

Electrical Characteristics Vcc = 5v + 5%, Vss = 0v, TA = 0 °C to 70 °C

Characteristic	Symbol	Min	Max	Units
MUX input high	TMH	60	110	ns
AEC setup time	TAEC	25	60	ns
MUX to RW setup or tri-state	TMRWS		70	ns
MUX to RW hold	TMRWH	30		ns
Up data setup from PH0	TMDS		130	ns
Up write data hold	THW	60		ns
Up data setup from Mux	TMXDS		120	ns
Data bus to tri-state from MUX	TMXDT	30		ns
Data bus to tri-state from AEC	TAEDT		120	ns
Read data stable	TDSU	40		ns
Read data hold	THR	40		ns
Address setup from PH0	TADS	40	150	ns
Address hold	THA	40		ns
Address setup from AEC	TAADS		75	ns
Address tri-state from AEC	TAEAT		120	ns
Port input setup	TPDSU	105		ns
Port input half	TPDH	65		ns
Port output data valid	TPDW		195	ns
Cycle time	TCYC	500		ns
PH0(in) pulse width @1.5v	PWHPH0	250	275	ns
PH0(in) rise time	TRPH0		10	ns
PH0(in) fall time	TFPH0		10	ns
RDY setup time	TRDY	80		ns

5.5.2 7501 TIMING DIAGRAM



6. DYNAMIC RAMS

This chapter covers the constraints and features of dynamic random access memories used in the TED system.

6.1 ELECTRICAL SPECIFICATIONS

INPUT VOLTAGE (Vin)	-1V to +7.0 VDC
SUPPLY VOLTAGE (Vcc)	-1V to +7.0 VDC
OPERATING TEMP (Ta)	0 to 70 'C
STORAGE TEMP	-55 to 150 'C
INPUT LEAKAGE CURRENT	-10.0 uA
DYNAMIC CHARACTERISTICS	Vcc = 5.0V +/-5%
INPUT HIGH VOLTAGE (VIH)	Vss+2.4V to Vcc+1V
INPUT LOW VOLTAGE (VIL)	VSS-1V to Vss+.8V
OUTPUT HIGH VOLTAGE (VOH) (IOH=-200uA VCC=4.75VDC)	VSS+2.4V
OUTPUT LOW VOLTAGE (VOL) (IOL=-4.2ma VCC=5.25V)	VSS+.4V
MAX POWER SUPPLY CURRENT	80ma

6.2 CHARACTERISTICS

This section covers some of the characteristics of the 64K by 1 bit RAM that is used in the TED 64 system.

6.2.1 PACKAGE PINOUT

PIN	NAME	DESCRIPTION
1	NC	
2	Din	DATA IN
3	/WE	WRITE ENABLE (ACTIVE LOW)
4	/RAS	ROW ADDRESS STROBE (ACTIVE LOW)
5	A0	ADDRESS BIT 0
6	A2	ADDRESS BIT 2
7	A1	ADDRESS BIT 1
8	VCC	POWER SUPPLY +5
9	A7	ADDRESS BIT 7
10	A5	ADDRESS BIT 5
11	A4	ADDRESS BIT 4
12	A3	ADDRESS BIT 3
13	A6	ADDRESS BIT 6
14	Dout	DATA OUT
15	/CAS	COLUMN ADDRESS STROBE (ACTIVE LOW)
16	VSS	POWER SUPPLY GROUND

6.2.2 SELECTION CRITERIA

The TED system uses low cost 200 ns access RAMs. Qualified parts must meet all timing parameters as specified in section 6.3.1 'TIMING CHART' and 6.3.2 'TIMING DIAGRAM'.

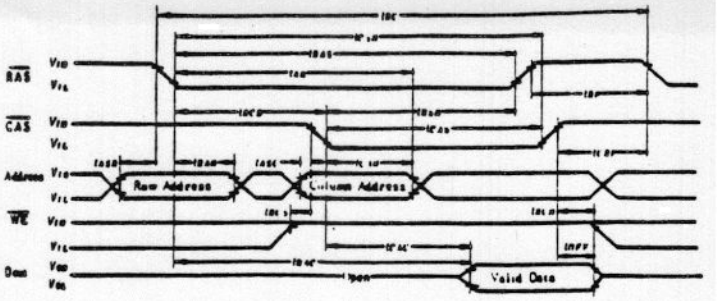
6.3 TIMING

This section illustrates the required timing constraints in dealing with DRAM.

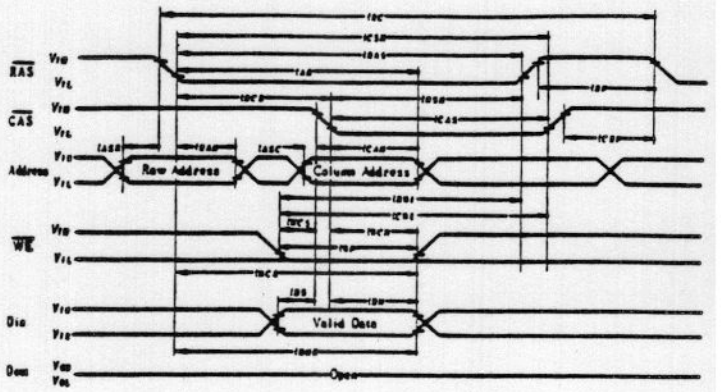
DRAM TIMING DIAGRAM

■ TIMING WAVEFORMS

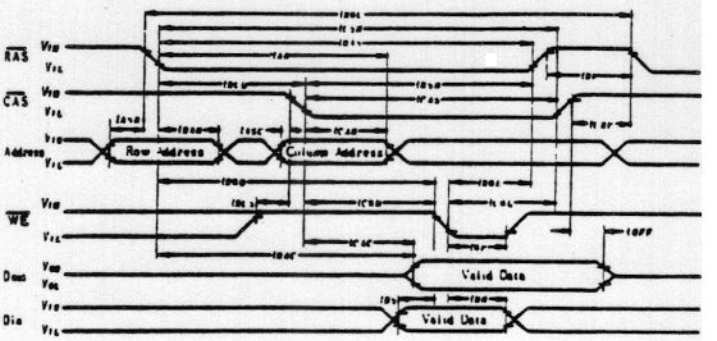
● READ CYCLE



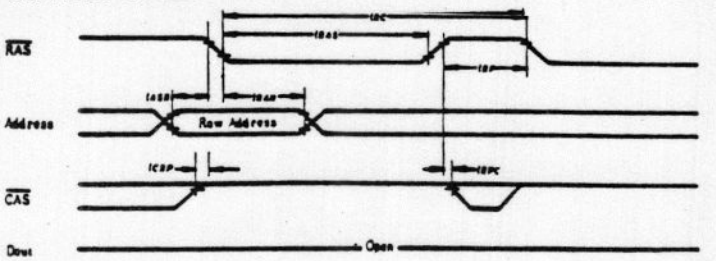
● WRITE CYCLE



● READ-WRITE/READ-MODIFY-WRITE CYCLE



● "RAS-ONLY" REFRESH CYCLE



7. THE USER PORT

This chapter details the system User Port.

7.1 DESCRIPTION

The USER PORT is included to allow various terminal and modem devices to connect to the TED system. Transmission and reception is via a 6551 ACIA, with handshaking assistance from a 6529 single port device. The 6551 and the 6529 are each accessable to the TED system in software, thus allowing their programming for various applications.

The 6551 ACIA is enabled by addresses $FD00 to $FD0F. The least significant two bits of the address will choose the mode, which may be set for transmit/recieve, recieve status, or programming of either the command register or the control register. Similarly, the 6529 is activated by the addresses $FD10 to $FD1F. It permits seven bits of either input or output, depending upon the status of the Read/Write line. The eighth bit, bit two to be exact, is used as the cassette sense input. It may be possible to utilize this bit if certain precautions are taken in software. (I.E. Insure that cassette sense is not grounded.)

The User Port itself provides access to various signals generated by these two chips, in addition to the ATN and Buffered Reset (BRESET) lines of the TED system. The port also provides ground, +5VDC and +9VAC for use by connected devices.

7.2 PHYSICAL PINOUT

PIN	NAME	DESCRIPTION	DIRECTION
A	GND	Ground	---------
B	P0	I/O Port Bit 0	Input/Output
C	RxD	Recieve Data	Input
D	RTS	Request to Send	Output
E	DTR	Data Terminal Ready	Output
F	P7	I/O Port Bit 7	Input/Output
H	DCD	Data Carrier Detect	Input
J	P6	I/O Port Bit 6	Input/Output
K	CTS	Clear to Send	Input
L	DSR	Data Set Ready	Input
M	TxD	Transmit Data	Output
N	GND	Ground	---------
1	GND	Ground	---------
2	+5	+5 VDC	---------
3	/BRESET	Buffered System Reset	Output
4	P2/CST SENSE	I/O Port Bit 2	Input/Output
5	P3	I/O Port Bit 3	Input/Output
6	P4	I/O Port Bit 4	Input/Output
7	P5	I/O Port Bit 5	Input/Output
8	RxC	Recieve Clock	Input/Output
9	ATN	Attention	Output
10	+9	+9 VAC	---------
11	+9	+9 VAC	---------
12	GND	Ground	---------

7.3 ELECTRICAL SPECIFICATIONS

I/O Ports (P0,P2..P7)

These ports are capable of driving up to four TTL type loads each in output configuration.

Buffered Reset (/BRESET)

The buffered reset line is capable of driving at least one TTL level load. It can drive a total of ten TTL loads between the User Port, the Serial Port, and the Expansion Port.

Attention (ATN)

This line is capable of driving at least one TTL level load. It can drive a total of ten TTL loads between the User Port and the Serial Port.

Recieve Data (RxD)

The Recieve Data input may be driven by a single TTL level driver.

Other Inputs (DCD, DSR, CTS)

The remaining data inputs are buffered by TTL buffers. Each may be driven by a single TTL level driver. CTS is sensed via 6529 under software control.

Recieve Clock (RxC)

The Recieve Clock, when acting as an output, can drive a single TTL level load. As an input, it must be driven by at least one TTL level load.

Transmit Data (TxD)

The Transmit Data output is capable of driving a single TTL level load.

Other Outputs (RTS, DTR)

The remaining outputs are each buffered by a TTL buffer, thus each of them will drive ten TTL level loads.

Five volt source (+5)

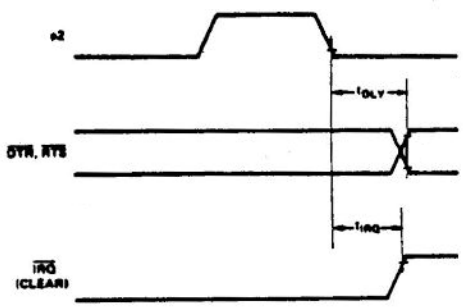
The five volt source is regulated DC, capable of supplying 100 mA worst case.

Nine volt source (+9)

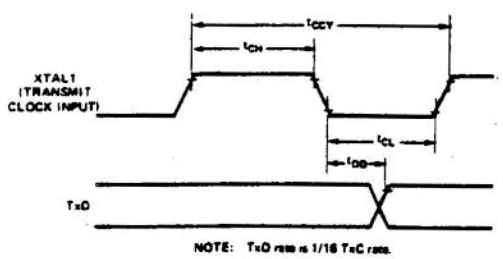
The nine volt source is an unregulated nine volt (RMS) supply, capable of supplying a worst case current of 400 DC mA.

7.4 TIMING

PARAMETER	SYMBOL	MIN	MAX	UNIT
Transmit/Receive Clock Rate	Tccy	400	-	ns
Transmit/Receive Clock High Time	Tch	175	-	ns
Transmit/Receive Clock Low Time	Tcl	175	-	ns
XTAL1 to TxD Propagation Delay	Tdd	-	500	ns
Propagation Delay (/RTS, /DTR)	Tdly	-	500	ns
/IRQ Propagation Delay (Clear)	Tirq	-	500	ns

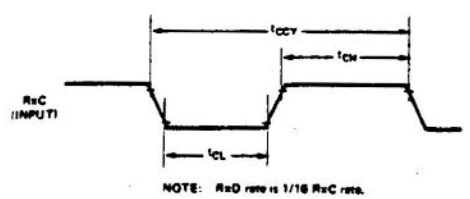


Interrupt and Output Timing



NOTE: TxD rate is 1/16 TxC rate.

Transmit Timing with External Clock



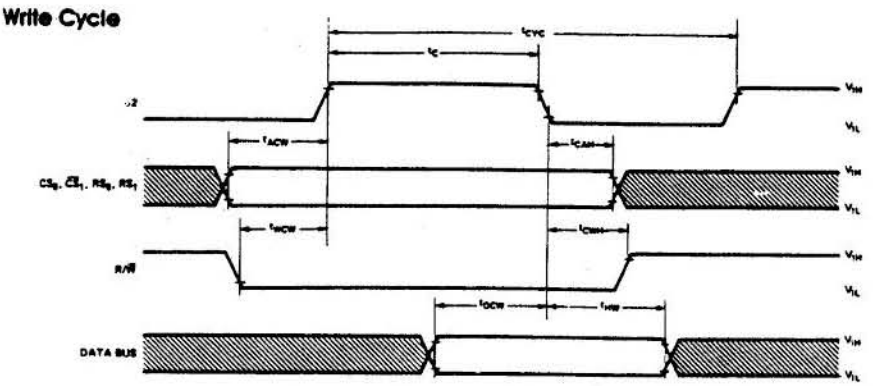
NOTE: RxD rate is 1/16 RxC rate.

Receive External Clock Timing

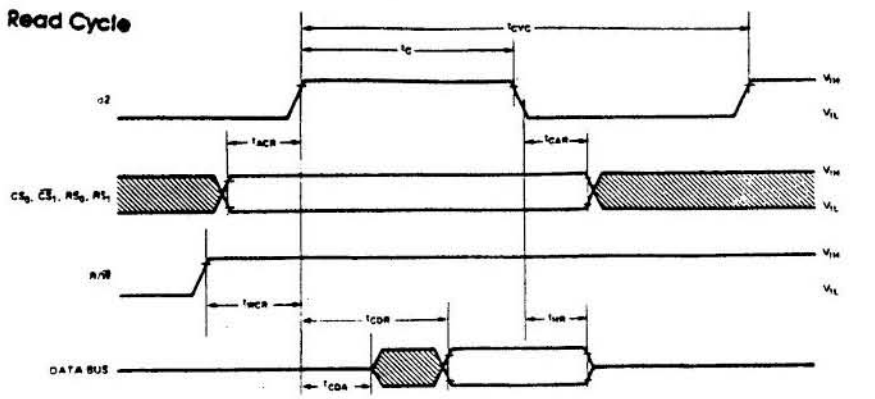
6551, 6529 TIMING

PARAMETER	SYMBOL	MIN	MAX	UNIT
PHI 2 PW	PW02	248	350	ns
ADDRESS SET UP TIME	TACR TACW	72	-	ns
ADDRESS HOLD	TCAH TCAR	25	-	ns
R/W SETUP	TWCW TWCR	71	-	ns
R/W HOLD	TCWH TWCR	93	-	ns
DATA BUS SETUP	TDCW	148	-	ns
READ ACCESS	TCDR	195	-	ns
READ DATA HOLD	THR	35	-	ns

Write Cycle



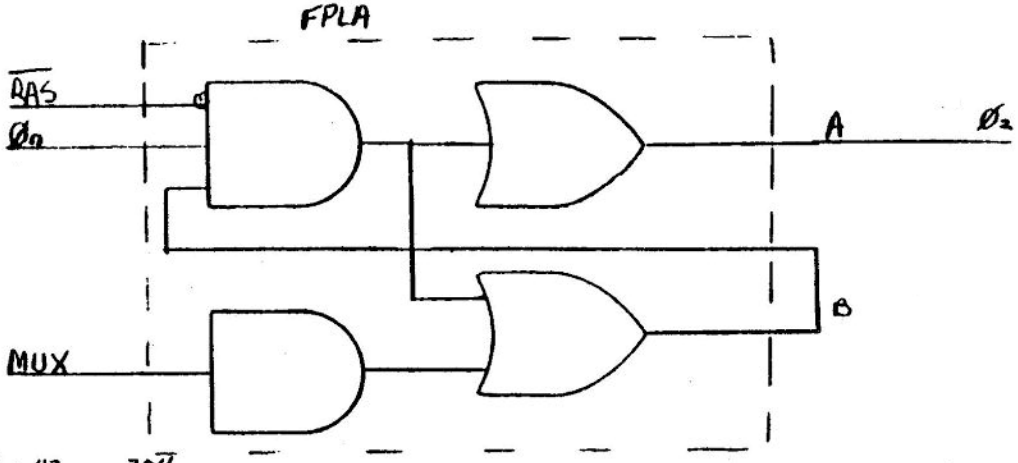
Read Cycle



PLA PROGRAM CHART

	PRODUCT TERM																ACTIVE LEVEL							
	INPUT VARIABLE																H	H	L	L	L	L	H	L
NUM	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OUTPUT FUNCTION							
																	7	6	5	4	3	2	1	0
0	-	-	-	-	-	-	-	H	-	-	-	-	-	-	-	-	A	.	.	.	.	.	.	.
1	L	-	-	-	-	-	-	-	-	-	-	-	-	-	H	H	A	.	.	.	.	.	A	.
2	-	H	H	H	L	H	H	-	H	L	L	L	L	H	H	-	.	.	.	.	A	.	.	.
3	L	H	H	H	L	H	H	-	H	L	L	L	H	H	H	H	.	.	.	.	.	A	.	.
4	L	H	H	H	L	H	H	-	H	L	L	H	H	H	H	H	.	.	A	.	.	.	.	.
5	-	H	H	H	L	L	H	-	H	-	-	-	-	H	-	-	.	A	.	.	.	.	.	.
6	L	H	H	H	L	H	H	-	H	H	H	L	H	H	H	H	.	.	.	A	.	.	.	.
7	L	H	H	H	L	H	H	-	H	L	L	H	L	H	H	-	.	.	.	.	.	.	.	A

ARM
KEYPORT $FD3X
KEYRN
KEYCLK
ADDR $FDDX
6552 $FDD0X
6552 $FDD1X
PHI2 CLK
SPEECH $FD2X



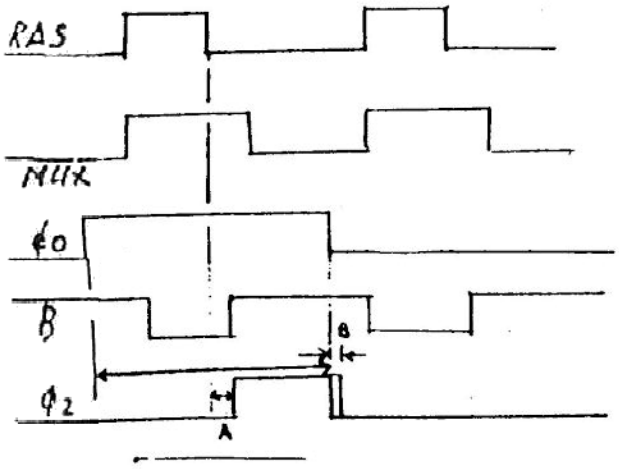
Ø0 to RAS L = 262 / Td Ø0 RAS L

RAS to Ø2 DELAY 17/42 To 7700 Td RAS Ø2 L

RAS to CS DELAY 17/42 RAS to Ø2 Td RAS CS L

Ø0 to CS DELAY 262 / Td Ø0 RAS L + 42 / Td RAS CS L = 304

Ø0 to Ø2 DELAY 17/42 To 7700 Td Ø0 Ø2 L



7.7 TED PHI 2 GENERATION

PLA INTERNAL LOGIC

UNLESS OTHERWISE SPECIFIED TOLERANCES ON: DECIMALS .X ± .XX ± .XXX ± ∠'S ±	DRAWN BY:	DATE	commodore
	CHKD:		Ø2 CLOCKS 64K TED
	ENGR:		
	APPR:		
MATERIAL:	USED ON	NEXT ASSY	SIZE / REV
FINISH:			SCALE / SHEET OF

8. THE VIDEO SECTION

8.1 VIDEO INTERFACE

The TED viedo interface hardware allows the connection of a standard NTSC or PAL commercial television and/or a color monitor. The monitor may accept either a composite video signal or separate chroma and luminance/sync signals in addition to an audio signal.

8.2 MODULATOR SPECIFICATIONS

The modulator provides a broadcast type RF signal carrying the composite video and audio signals. The NTSC modulator is switchable between channels 3 and 4 to help minimize local broadcast interference. The signal generated by the RF modulator complies with FCC ruling concerining FCC Class B, TV Interface Devices.

8.3 MONITOR OUTPUT

The monitor output provides the following signals:

Luminance/Sync	1 V p-p	75 ohms
Chroma	1 V p-p	75 ohms
Audio	1 V p-p	
Composite	1 V p-p	75 ohms

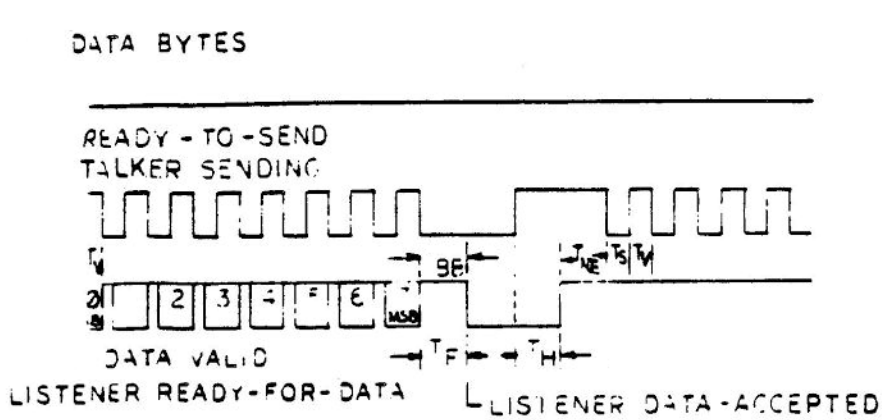
8.4 VIDEO CONNECTOR PINOUT

The video connector provides the following signals:

PIN	SIGNAL
1	Luminance/Sync
2	Ground
3	Audio Out
4	Composite
5	Audio In
6	Chroma
7	N.C.
8	N.C.

9. THE SERIAL BUS

9.1 SERIAL BUS SPECIFICATION

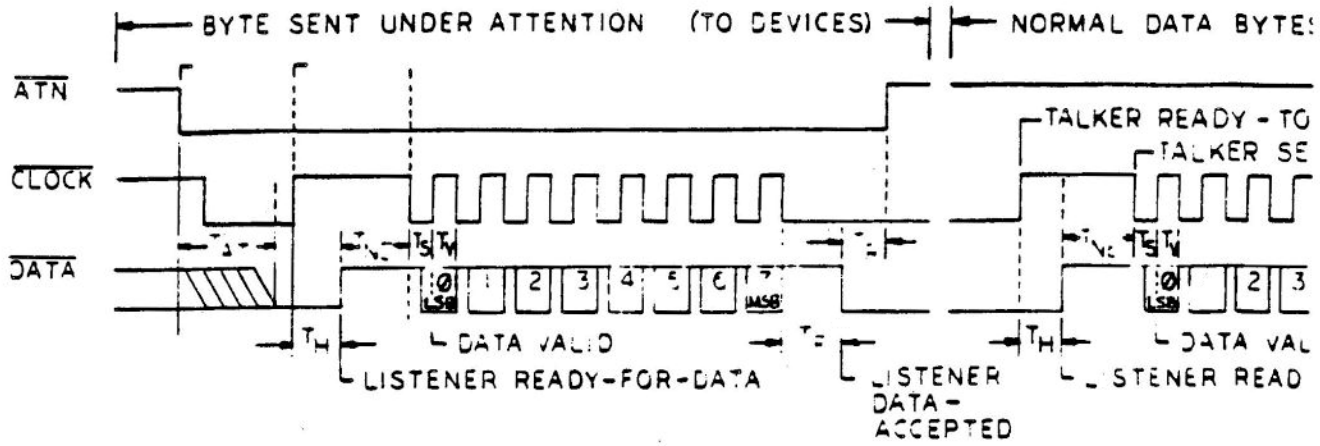


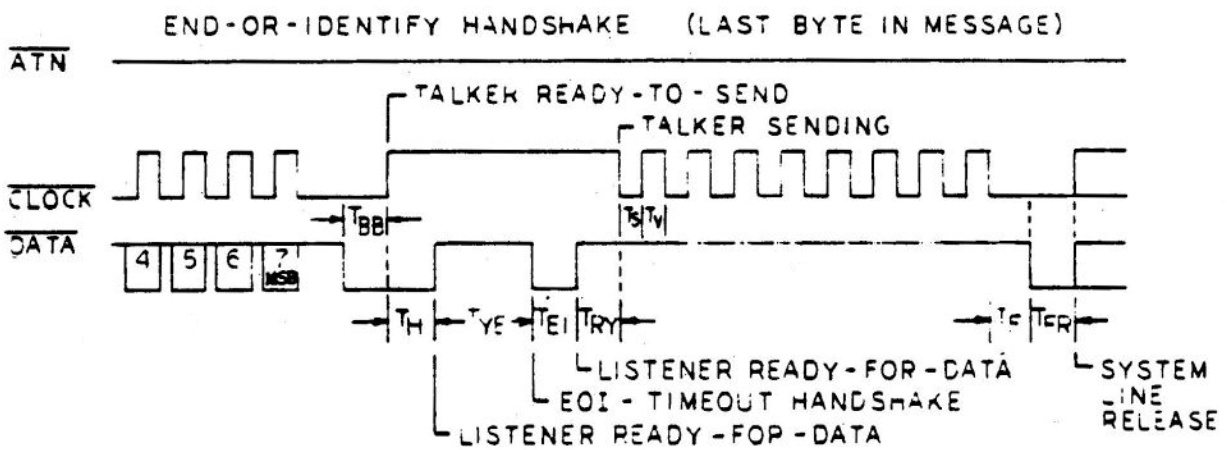
SERIAL BUS TIMING

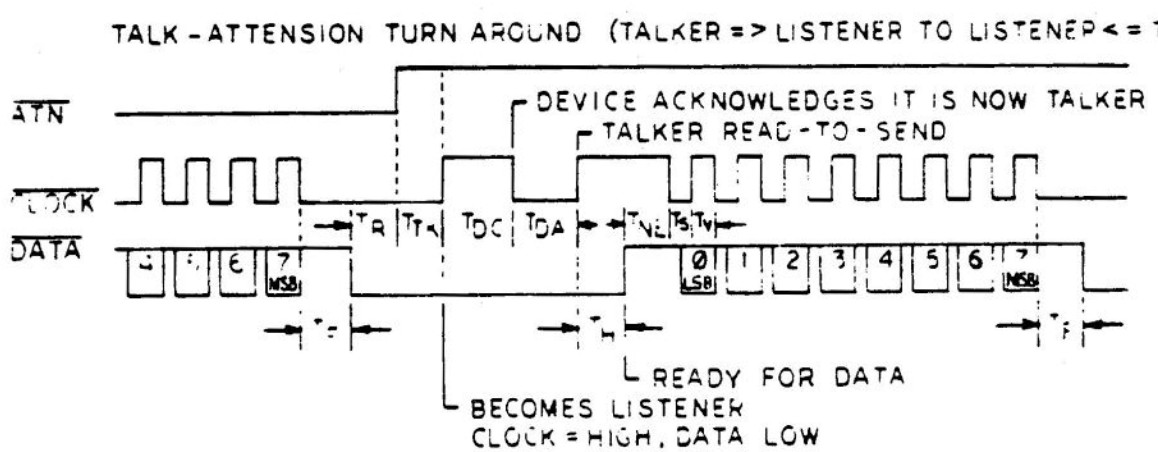
	SYMBOL	MIN	TYP	MAX.
ATN RESPONSE (REQUIRED) ①	T_{AT}	—	—	1000 μs
LISTENER HOLD-OFF	T_H	0	—	∞
NON-EOI RESPONSE TO RFD ②	T_{NE}	—	40 μs	200 μs
BIT SET-UP TALKER ④	T_S	20 μs	70 μs	—
DATA VALID	T_V	20 μs	20 μs	—
FRAME HANDSHAKE ③	T_F	0	20	1000 μs
FRAME TO RELEASE TO ATN	T_R	20 μs	—	—
BETWEEN BYTES TIME	T_{BB}	100 μs	—	—
EOI RESPONSE TIME	T_{YE}	200 μs	250 μs	—
EOI RESPONSE HOLD TIME ⑤	T_{EI}	60 μs	—	—
TALKER RESPONSE LIMIT	T_{RY}	0	30 μs	60 μs
BYTE-ACKNOWLEDGE ④	T_{PR}	20 μs	30 μs	—
TALK-ATTENSION RELEASE	T_{TK}	20 μs	30 μs	100 μs
TALK-ATTENSION ACKNOWLEDGE	T_{DC}	0	—	—
TALK ATTENSION ACK. HOLD	T_{DA}	50 μs	—	—
EOI ACKNOWLEDGE	T_{FR}	60 μs	—	—

⑤ T_{EI} MIN. MUST BE 80 μs FOR EXTERNAL DEVICE TO BE A TALKER.
④ T_V AND T_{PR} MIN MUST BE 60 μs FOR EXTERNAL DEVICE TO BE A TALKER.
③ IF MAX. TIME EXCEEDED, FRAME ERROR.
② IF MAX. TIME EXCEEDED, EOI RESPONSE REQUIRED.
① IF MAX. TIME EXCEEDED, DEVICE NOT PRESENT ERROR.

NOTES:


BYTE SENT UNDER ATTENTION (TO DEVICES)
NORMAL DATA BYTE
ATN
CLOCK
DATA
TALKER READY - TO
TALKER SE
DATA VALID
LISTENER READY-FOR-DATA
LISTENER
DATA -
ACCEPTED
DATA VAL
STENER READ

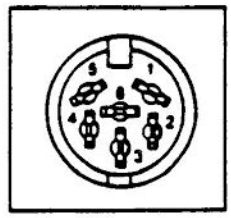

END-OR-IDENTIFY HANDSHAKE (LAST BYTE IN MESSAGE)
ATN
CLOCK
DATA
TALKER READY-TO-SEND
TALKER SENDING
LISTENER READY-FOR-DATA
EOI - TIMEOUT HANDSHAKE
LISTENER READY-FOR-DATA
SYSTEM
INE
RELEASE


TALK-ATTENSION TURN AROUND (TALKER => LISTENER TO LISTENER <= TALKER)
ATN
DATA
DEVICE ACKNOWLEDGES IT IS NOW TALKER
TALKER READ-TO-SEND
READY FOR DATA
BECOMES LISTENER
CLOCK = HIGH, DATA LOW

9.1 CONT

9.2 SERIAL BUS CONNECTOR PINOUT

Pin	Type
1	SERIAL $\overline{\text{SRQIN}}$
2	GND
3	SERIAL ATN IN/OUT
4	SERIAL CLK IN/OUT
5	SERIAL DATA IN/OUT
6	$\overline{\text{RESET}}$



10. THE EXPANSION BUS

10.1 EXPANSION BUS PINOUT

PIN	NAME	PIN	NAME
1	GND	A	GND
2	+5	B	C1LOW
3	+5	C	/BRESET
4	/IRQ	D	/RAS
5	R/W	E	PHI0
6	C1HI	F	A15
7	C2LOW(reserved)	H	A14
8	C2HI(reserved)	J	A13
9	/CS1	K	A12
10	/CS0	L	A11
11	/CAS	M	A10
12	MUX	N	A9
13	BA	P	A8
14	D7	R	A7
15	D6	S	A6
16	D5	T	A5
17	D4	U	A4
18	D3	V	A3
19	D2	W	A2
20	D1	X	A1
21	D0	Y	A0
22	AEC	Z	NC
23	EXT AUDIO	AA	NC
24	PHI 2	BB	NC
25	GND	CC	GND

10.2 EXPANSION CONNECTOR SIGNAL DESCRIPTION

A0 - A15	SYSTEM ADDRESS BUS - UNBUFFERED. OUTPUT.
D0 - D7	SYSTEM DATA BUS -UNBUFFERED. OUTPUT.
/CS0,/CS1	INTERNAL ROM CHIP SELECTS. OUTPUT.
C1LOW,C1HI	EXTERNAL CARTRIDGE CHIP SELECTS. ACTIVE LOW. OUTPUT.
/RAS	DRAM ROW ADDRESS STROBE. OUTPUT.
MUX	DRAM ADDRESS MULTIPLEX CONTROL SIGNAL. OUTPUT.
/CAS	DRAM COLUMN ADDRESS STROBE. OUTPUT.
BA	BUS AVAILABLE. LOW FOR DMA. OUTPUT ONLY.
PHI 2	ARTIFICIAL PHI 2. ADDRESS VALID RISING EDGE. DATA VALID FALLING EDGE. OUTPUT.
R/W	SYSTEM READ WRITE LINE. OUTPUT.
/IRQ	INTERUPT REQUEST. INPUT.
/BRESET	BUFFERED RESET. OUTPUT.
EXT AUDIO	EXTERNAL AUDIO. INPUT. 1 V P-P FULL SCALE. AC COUPLED.

11. READ ONLY MEMORY

11.1 SYSTEM ROM DESCRIPTION

In a basic configuration, the TED operating system resides in 32K of read only memory contained in two 16K X 8 ROM. The KERNAL resides in the upper 16K ROM (referred to as HIGH ROM) and some of the lower 16K ROM (LOW ROM). The Kernal, by definition, is the operating system of the computer, with fixed entry points into usable subroutines to facilitate use by higher level programs. The entry table for the Kernal is located above the 7360 in memory. ($FF40 - $FFF9) Contained in the space allocated for the Kernal is the character ROM at location $D000 - $D7FF. 'BASIC' is contained in the lower ROM not used by the Kernal.

11.2 BANKING ROM OPERATION

Although the system can only 'see' 32K of ROM at a time, up to 64K can be installed on board, with an additional 32K on as external cartridge. This is possible using the scheme known as 'banking'. Banking is accomplished by writting to thee address range of $FDD0 - $FDDF. When a write to this address range occurs, the lower four bits of the address bus select 2 of 8 banks (each 16K). Refer to the chart below.

A0	A1	BANK
0	0	low internal #1, 'BASIC'
0	1	low internal #2, 'FUNCTION LOW'
1	0	low external #1, 'CARTRIDGE LOW'
1	1	reserved

A2	A3	BANK
0	0	hi internal #1, 'KERNAL'
0	1	hi internal #2, 'FUNCTION HI'
1	0	hi external #1, 'CARTRIDGE HI'
1	1	reserved

Even when the Kernal is banked out, part of the Kernal remains accessable. This is the part of the Kernal that does the actual banking and is loacted in the address range of $FC00 to $FCFF. This section of ROM will not assert itself if ROM is banked out for RAM.

11.3 ROM ELECTRICAL SPEC

Absolute Maximum Ratings

INPUT VOLTAGE (Vin)	-.5V to +7.0 VDC
SUPPLY VOLTAGE (Vcc)	-.5V to +7.0 VDC
OPERATING TEMP (Ta)	0 to 70 'C
STORAGE TEMP	-55 to 150 'C

D.C. Characteristics

INPUT LEAKAGE CURRENT	-10 uA
DYNAMIC CHARACTERISTICS	Vcc = 5.0V +/-5%
INPUT HIGH VOLTAGE (VIH)	Vss+2.4V to Vcc+1V
INPUT LOW VOLTAGE (VIL)	VSS-.5V to Vss+.8V
OUTPUT HIGH VOLTAGE (VOH) (IOH=-200uA VCC=4.75VDC)	VSS+2.4V
OUTPUT LOW VOLTAGE (VOL) (IOL=-3.2ma VCC=5.25V)	VSS+.4V
MAX POWER SUPPLY CURRENT	120 mA

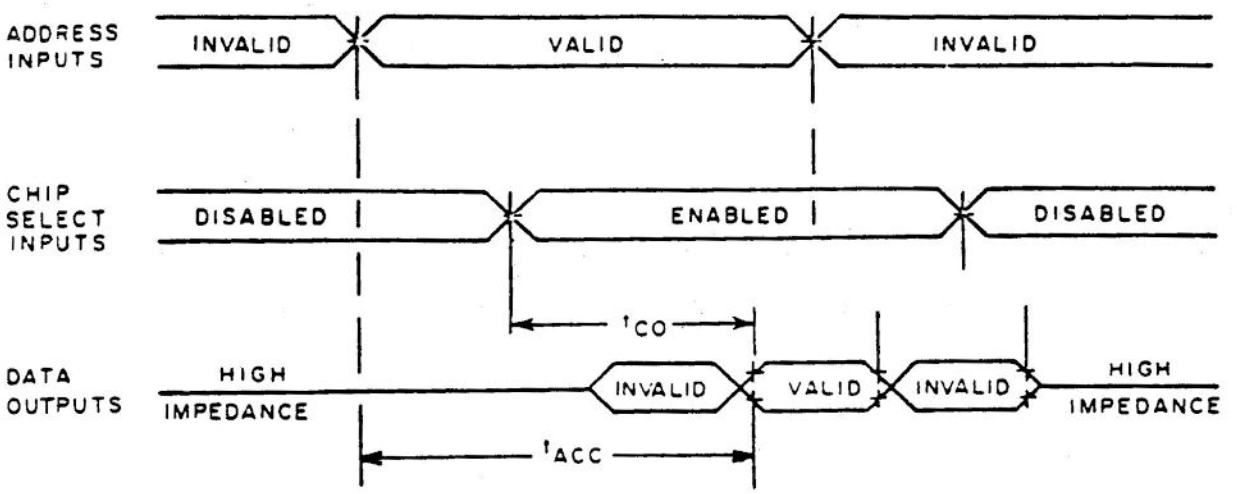
11.4 23128 ROM PINOUT

PIN	NAME	DESCRIPTION
1	NC	
2	A12	ADDRESS BIT 12
3	A7	ADDRESS BIT 7
4	A6	ADDRESS BIT 6
5	A5	ADDRESS BIT 5
6	A4	ADDRESS BIT 4
7	A3	ADDRESS BIT 3
8	A2	ADDRESS BIT 2
9	A1	ADDRESS BIT 1
10	A0	ADDRESS BIT 0
11	D0	DATA BIT 0
12	D1	DATA BIT 1
13	D2	DATA BIT 2
14	GND	POWER SUPPLY GROUND
15	D3	DATA BIT 3
16	D4	DATA BIT 4
17	D5	DATA BIT 5
18	D6	DATA BIT 6
19	D7	DATA BIT 7
20	/CS	CHIP SELECT / ACTIVE LOW
21	A10	ADDRESS BIT 10
22	/CE	CHIP ENABLE / ACRTIVE LOW
23	A11	ADDRESS BIT 11
24	A9	ADDRESS BIT 9
25	A8	ADDRESS BIT 8
26	A13	ADDRESS BIT 13
27	CS or CE	CHIP SELECT OR CHIP ENABLE / ACTIVE HIGH
28	VCC	POWER SUPPLY +5

11.5 ROM TIMING SPECIFICATION

PARAMETER	SYMBOL	MIN.	MAX.	
ACCESS TIME	TACC	300	-	ns
OUTPUT ENABLE	TOE	120	-	ns

Note: TACC available from system is 338ns and TOE available is 120ns.

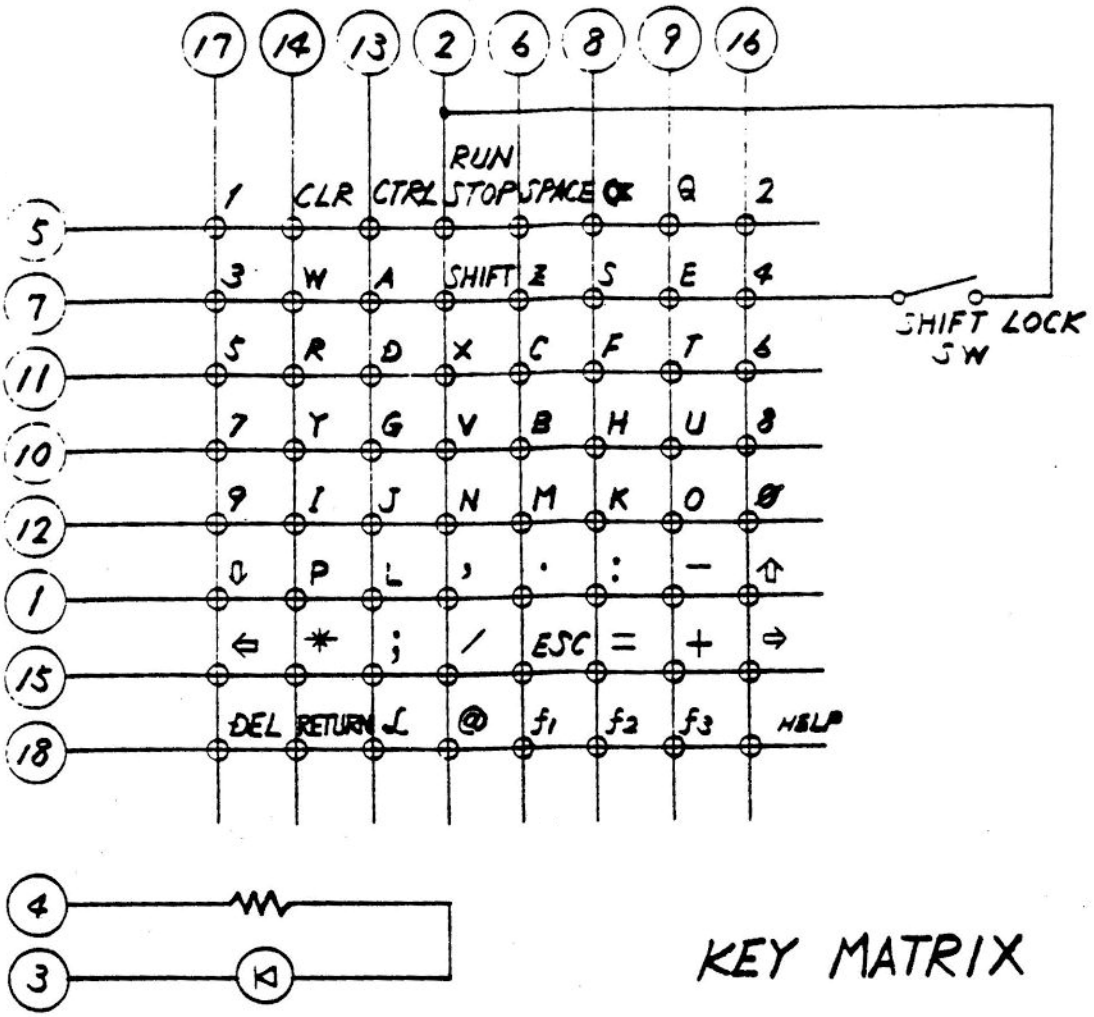


12. THE KEYBOARD

12.1 KEYBOARD CONNECTOR PINOUT

PIN	NAME	DESCRIPTION
1	D5	DATA BIT 5
2	K7	KEY LATCH BIT 7
3	GND	LED GND
4	+5V	LED +5VOLT 20ma MAX.
5	D7	DATA BIT 7
6	K4	KEY LATCH BIT 4
7	D1	DATA BIT 1
8	K5	KEY LATCH BIT 5
9	K6	KEY LATCH BIT 6
10	D3	DATA BIT 3
11	D2	DATA BIT 2
12	D4	DATA BIT 4
13	K2	KEY LATCH BIT 2
14	K1	KEY LATCH BIT 1
15	D6	DATA BIT 6
16	K3	KEY LATCH BIT 3
17	K0	KEY LATCH BIT 0
18	D0	DATA BIT 0

12.2 KEYBOARD MATRIX



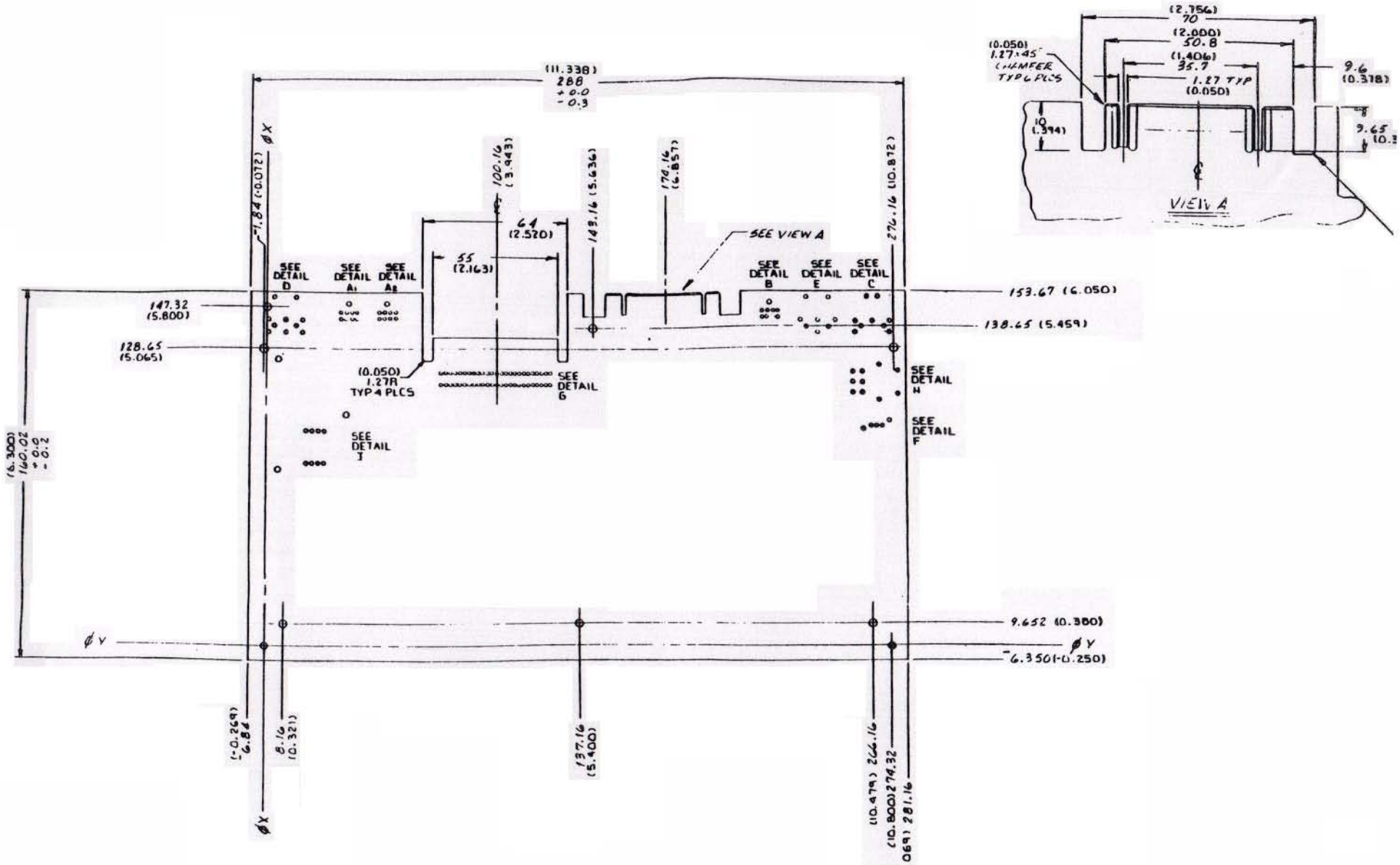
KEY MATRIX

12.3 KEYBOARD ELECTRICAL SPECIFICATION

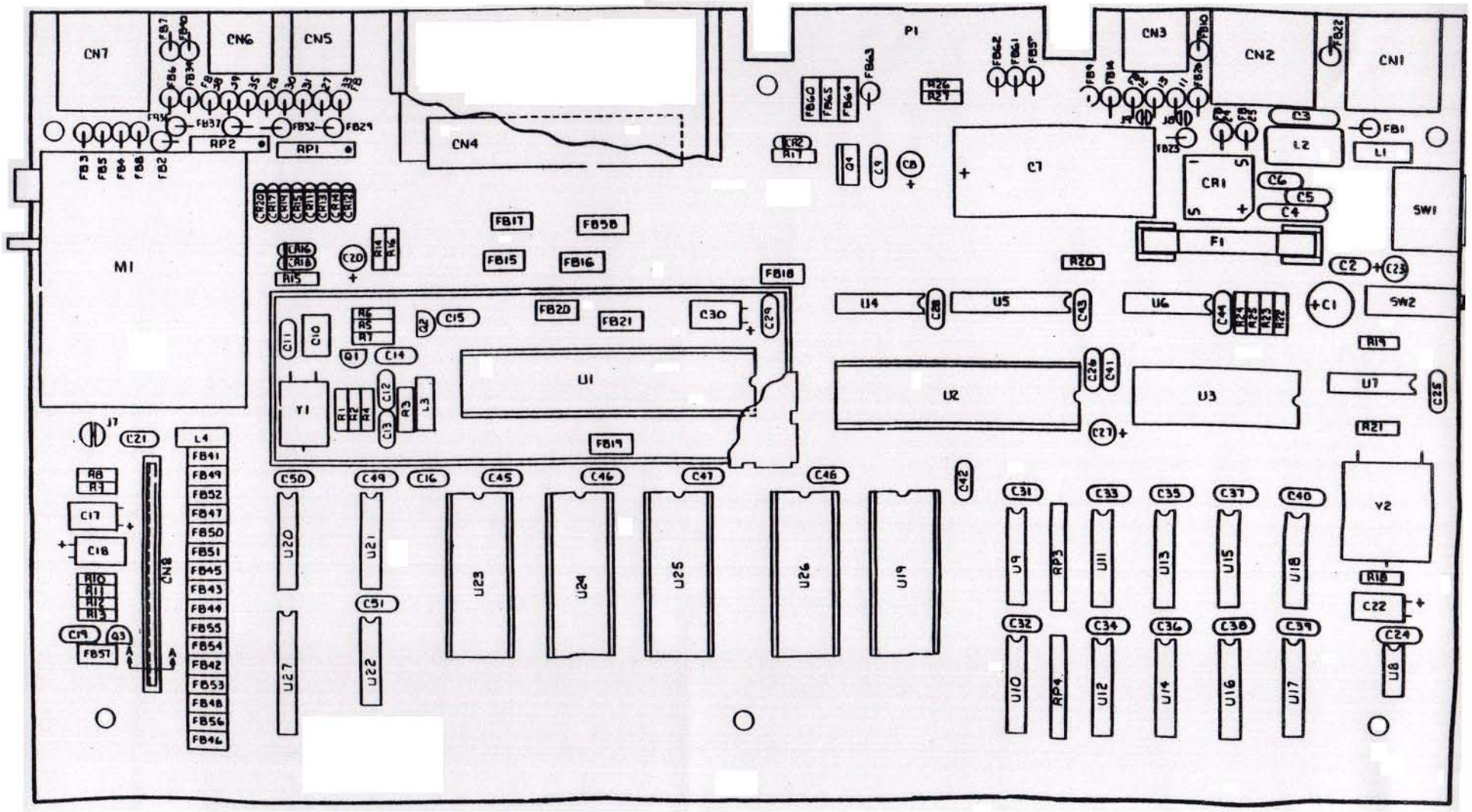
1)	MAXIMUM RATING	12VDC, 200uS PULSE WIDTH 1/5Ω DUTY CYCLE 1ma
2)	CHATTERING	5mSEC INITIAL, 10mSEC OVER LIFE
3)	CONTACT RESISTANCE	500 OHM MAX.
4)	CAPACITANCE	100pf MAX
5)	INSULATION RES.	50M OHM MIN.
6)	WITHSTAND VOLTAGE	250VAC 1min.
7)	OPERATING FORCE	65g TYP.
	ZERO TRAV FORCE	15+/-10g AT .5mm TRAV
	FULL TRAV FORCE	90+/-25g AT .5mm ABOVE FULL TRAV
8)	OPERATING LIFE	500 MILLION TIMES
	FUNCTION KEYS	300 MILLION TIMES
9)	OPERATING TEMP	-5 - +50 'C
10)	STORAGE TEMP	-20 - +65'C

13. THE CIRCUIT BOARD

13.1 PHYSICAL DIMENSIONS



13.2 PARTS PLACEMENT



CLOCKS

PARAMETER	SYMBOL	MIN	MAX	UNIT	REFERENCE SHEET	SYNONYM	EQUATION
CYCLE TIME, Single speed	TCYCS	117	139	ns	A	TRC	
CYCLE TIME, Double speed	TCYCD	559	559	ns	A	TRC	
Pulse Width Phi Low (SS)	PwØLS	515	585	ns	A		
Pulse Width Phi High (SS)	PwØHS	515	585	ns	A		
Pulse Width Phi Low (DS)	PwØLD	275	295	ns	A		
Pulse Width Phi High (DS)	PwØHD	260	285	ns	A		
I/O to AEL Relay	TAEC	10	40	ns	B		
PHI LOW TO RAS HI	TdØLRH	60	110	ns	A	TdCoRH	
PHI LOW TO RAS LOW	TdØLRL	220	260	ns	A	TdCoRL	
RAS HI Width RAS PRECHARGE	TRP	120	200	ns	A	TRH	
RAS LOW WIDTH	TRAS	359	439	ns	A	TRL, TCSH	
PHI HI TO CAS HI PHI HI TO RAS HI PHI HI TO MUX HI	TdØHCH TdØHRH TdØHMH	60	110	ns	A	TdCoRH	
PHI HI TO RAS LOW	TdØHRL	220	260	ns	A	TdCoRL	
PHI LOW TO MUX HI	TdØLMH	60	110	ns	A	TdCoMH	
PHI LOW TO MUX LOW	TdØLML	260	290	ns	A	TdCoML	
MUX HI Pulse width	TMH	120	-	ns			
MUX LOW Pulse width	TML	299	-	ns			
RAS LOW TO MUX LOW	TRLML	20	-	ns	A	TRM	
MUX LOW TO CAS LOW	TMLCL	35	-	ns	A	TMC	
PHI LOW TO CAS HI	TdØLCH	60	110	ns	A	TdCoCH	
CAS HI Pulse width (READ)	TCHR	200		ns	A	TCH(READ)	
CAS HI Pulse width (WRITE)	TCHW	275		ns		TCH(WRITE)	
PHI LOW TO CAS LOW (READ)	TdØLCLR	300	365	ns	A	TdCoCL	
CAS LOW to PHI HI (WRITE)	TCLØHW	0	100	ns	A	TCL	
CAS LOW TO PHI HI READ	TCLØHR	205	—	ns	A		
CAS LOW TO PHI HI WRITE	TdCLØHW	75	—	ns	A		
RAS LOW TO CAS LOW	TRCD	75	—	ns	A	TRC, TRLCL	
CAS HI TO RAS LOW CAS TO RAS PRECHARGE	TCRP	-120	—	ns	A		TCRP = TRP
PHI HI DOUBLE SPEED TO CAS (WRITE)	TWCS	130	-	ns			
RAS LOW TO PHI HI	TdRLØH	240	—	ns			
RAS LOW TO PHI LOW	TRLØL	290	—	ns			
RAS LOW TO PHI LOW DOUBLE SPEED	TRLØLD	250	—	ns			
CAS LOW TO PHI LOW READ Double Speed	TdCLØLRD	185	—	ns			
CAS LOW TO PHI LOW WRITE Double Speed	TdCLØLWD	88	—	ns			
CAS LOW TO PHI LOW (READ)	TCLØLR	205	—	ns			
CAS LOW TO PHI LOW (WRITE)	TdCLØLW	75	—	ns			
CAS LOW Pulse width (WRITE)	TCASW	140		ns			
CAS LOW Pulse width (READ)	TCASR	219	—	ns			
RAS LOW TO PHI2 LOW	TdRLØ2	17	42	ns			TP 1700
RAS LOW TO CS	TdRLCS	17	42	ns			TP 1700
PHI LOW TO PHI2 LOW	TdØLØ2	17	42	ns			TP 1700
PHI LOW TO CS HI	TdØLCS	17	42	ns			TP 1700
PHI HI TO PHI 2 HI	TdØHØ2H	237	302	ns			TdØHRL + TRLØ2L
PHI 2 PULSE WIDTH	PwØ2	260	298	ns			PwØ2S = TdØLØ2 - TdØHØ2H NOTE: TP7700 DOES NOT AGREE WITH THIS EQN
PHI HI Double Speed to PHI2	TdØDSØ2H	17	42	ns			TP 1700

ROM

PARAMETER	SYMBOL	MIN	MAX	UNITS	FIGURE(#)	EQUATION
Access Time (ADDRESS)	ROM TACC	–	335	ns		PWQL - TADS - TOSD
Access Time (chip select)	TDE	–	118	ns	TCO	PWØL - TCS5 - TPHA5139 - TOSD MARGIN -2

7360 TED

PARAMETER	SYMBOL	MIN	MAX	UNIT	REFERENCE SHEET	SYNONYM	NOTES & EQUATIONS
TED ADDRESS SETUP	TADS	—	150	nS	TED SPEC		
INPUT DATA STABLE	TDSU TED	90	—	nS	TEDSPEC	TDSU	
INPUT DATA HOLD	TDH	10	—	nS	TED SPEC	TOH1	
OUTPUT DATA STABLE	TDCO1	160	—	nS	TED SPEC		
OUTPUT DATA HOLD	TD HO	80	120	nS	TED SPEC		
R/W STABLE PERIOD	TRWS	—	178	nS			$T_{MRWS} + T_{d\phi HMH}$
MUX TO R/W SETUP OR TRISTATE	TMRWS	—	70	nS	7501 SPEC		
MUX TO R/W HOLD	TMRWH	30	—	nS	7501 SPEC		
CHIP SELECT SETUP	TCSS	—	305	nS			$P_W\phi_{LX} - T_{OSU\,TED} - ROM\,TOE$
CHIP SELECT HOLD	TCSH	40	110	nS			
ADDRESS HOLD	TAH	40	—	nS			
ADDRESS IN TRI-STATE	TADTH	—	?				$T_{AADS} + TATC$

7501

DOC C

PARAMETER	SYMBOL	MIN	MAX	UNIT	REFERENCE SHEET	SYNONYM	NOTES & EQUATIONS
ADDRESS SETUP F/ PHØ	TADS	40	150	nS	7501 SPEC		
ADDRESS HOLD	TAH	40	—	nS	7501 SPEC	THA	
ADDRESS SETUP F/ AEC	TAADS	—	75	nS	7501 SPEC		SINGLE SPEED
ADDRESS TRI-STATE F/$\overline{AEC}$	TAEAT	—	120	nS	7501 SPEC		SINGLE SPEED
$\overline{MUX}$ INPUT HIGH	TdØLMH	60	110	nS	7501 SPEC	Tmm	
AEC SETUP TIME	TAEC	25	60	nS	7501 SPEC		SINGLE SPEED
$\overline{MUX}$ TO RW SETUP OR TRISTATE	TMRWS	—	70	nS	7501 SPEC		
$\overline{MUX}$ TO RW HOLD	TMRWH	30	—	nS	7501 SPEC		
DATA SETUP FROM PHØ	TmDS	—	130	nS	7501 SPEC		DOUBLE SPEED
DATA SETUP FROM $\overline{MUX}$	TMXDS	—	120	nS	7501 SPEC		SINGLE SPEED
DATA BUS IN TRISTATE FROM $\overline{MUX}$	TMXDT	30	—	nS	7501 SPEC		SINGLE SPEED
DATA BUS TO TRISTATE FROM $\overline{AEC}$	TAEDT	—	120	nS	7501 SPEC		
READ DATA STABLE	TDSU 7501	40	—	nS	7501 SPEC	TDSU	
READ DATA HOLD	TOFF	40	—	nS	7501 SPEC	THR	
WRITE DATA HOLD	THW	60	—	nS	7501 SPEC		
READ/WRITE STABLE	TRWS	—	193	nS	CLKS, 7501		TMRWS + TdØHMH

6551A TIMING

DOC D

PARAMETER	SYMBOL	MIN	MAX	UNIT	SHEET	SYNONYM	EQUATION	
CLOCK CYCLE TIME	TCYC	558	1118	nS		TCYCS, TCYCD		
ϕ_2 PULSE WIDTH	PWϕ2	460	390	nS	CLOCKS	Tc	PWϕH S+ Td $\phi_{nL\phi_2}$ - Td$\phi_{L\phi_2}$	
ADDRESS SETUP TIME	TAC 6551 TASR	87	—	nS		TACW	Td $\phi_{nH\phi_2}$ - TADS - TP7700	
ADDR HOLD TIME	TCAH 6551 TCAR	-2	—	nS	CLKS, 7501	TCAH	TAH - Td$\phi_{L\phi_2}$	* NEG MARGINAL
R/W SET-UP TIME	TWCW TWCR	87	—	nS	CLKS, 7501		Td $\phi_{nH\phi_2}$ - TRWS	
R/W HOLD TIME	TCW H TWCR	93	—	nS	CLKS, 7501		Tdϕ_{LMH} + TWRW H	
DATA [illegible]	TDCW	197	-	nS	CLKS, 7501		PWϕ_{nH} + TDC, DSL - TDDS	
READ ACCESS TIME	TCDR	178	-	nS	CLKS, 7501		TcRLϕ_2 + Td R$_{L\phi_2}$ - TDSU	
READ DATA HOLD	THR	37	—	nS			Td $\phi_{LL\phi_2}$ + THR 6551	* NEG MARGINAL
DOUBLE SPEED								
ϕ_2 PULSE WIDTH	PWϕ_2	≈ 274					PWϕ_{nH} DS + TP7700 - TP7700	
ADDR SETUP TIME	TACW 6551 TASR	141					PWϕ_{LDS} - TADS + TP7700	
ADDR HOLD TIME	TCAH 6551 TACR	-2						* NEG MARGIN
R/W SET UP TIME	TWCW TWCR	102					PWϕ_{L} - TRWS + TP7700	
R/W HOLD		93						
DATA SETUP	TDCW	61						
READ ACCESS	TCDR	178					PWϕ_{HDS} - TP7700(MAX) - TDSU 6510	
READ DATA HOLD	THR	37						

6529 TIMING

PARAMETER	SYMBOL	MIN	MAX	UNIT	SHEET	SYNONYM	EQUATION
WRITE ACTIVE	TWA	222.5	—	ns	CLOCKS		$T_{dR_L\phi_L} + T_d\phi_L C_S - T_{dR_L C_S}$
$\overline{CS}$ TO PORT OUT DELAY	TCPD	—	500	ns	6529 REF		
DATA TO $\overline{CS}$ SETUP	TDS	148	—	ns	CLOCKS		$P_{W\phi_H D} + T_d\phi_L \phi_{2L} - T_{mOS}$
DATA TO $\overline{CS}$ HOLD	TDH	10		ns	CLKS, 7501		$T_{OFF} - T_d \phi_L C_S$
ACCESS TIME	TACC	—	234	ns	CLKS, 7501		$T_{dR_L\phi_L} - T_{dR_L C_S} - T_{DSU}$ 7501
R/$\overline{W}$ TO $\overline{CS}$ SETUP	TRWS 6529	152	—	ns	CLKS, 7501		$P_{W\phi H D} - T_{RWS} - T_d C_L \phi_L$
R/$\overline{W}$ TO $\overline{CS}$ HOLD	TRWH 6529	79.5	—	ns	CLKS, 7501		$T_{CYC R} + T_{MRW H} - T_{WA\ 6529}$
$\overline{CS}$ TO OUTPUT OFF DELAY	TOTD	20	120	ns	6529 REF		

DRAMS

DOC F

PARAMETER	SYMBOL	MIN	MAX	UNIT	REFERENCE SHEET	SYNONYM		EQUATION
RANDOM CYCLE TIME	TRC	558	1118	ns	CLOCKS	TCKS, TCYCD		Tcycs
ACCESS TIME F/RAS	TRAC	–	20					TdRLØ2 – TDSU (WC …)
ACCESS TIME F/CAS	TCAC	–	115					TCAC SPEC'D BY TED's NEG MARGIN X TO BE ADDRESED BY NEXT REV TEL
TURN OFF DELAY	TOFF	0	40	ns	SEE DRAM DATA SHEET, APPROX only			
RAS PRECHARGE TIME	TRP	120	–	ns	CLOCKS	TRH		TRP = TRH
RAS PULSE WIDTH	TRAS	359	–	ns	CLOCKS	TRL		TRAS = TRL
RAS HOLD TIME (READ)	TRSHR	279	–	ns		TCL		Td ØxRH = Td Ø2CH, TRSHR = TCASR
RAS HOLD TIME (WRITE)	TRSHW	149	–	ns	CLOCKS	TCL, TAS		Td ØxRH = Td ØxCH, TRSHW = TCASW
CAS PULSE WIDTH (READ)	TCASR	279	–	ns	CLOCKS			(DEFINED ON CLOCKS SHEET)
CAS PULSE WIDTH (WRITE)	TCASW	149	–	ns	CLOCKS	TCL, TCAS		(DEFINED ON CLOCKS SHEET)
CAS HOLD TIME	TCSH	359	–	ns	CLOCKS	TRAS, TRL		Td ØxRH = Td ØxCH, TCSH = TRAS
RAS TO CAS DELAY TIME	TRCD	75	–	ns	CLOCKS	TRC		(DEFINED ON CLOCKS SHEET)
CAS TO RAS PRECHARGE	TCRP	85	–	ns	CLOCKS			Td ØxRH = Td ØxCH, TCRP = TRP
ROW ADDR SETUP TIME	TASR	46	–					Td ØxRL – Tpl S257 DATA – TADS
ROW ADDR HOLD TIME	TRAH	24	–	ns				Td RLML (min) + Tpl S257 SEL (min)
COL ADDR SET-UP	TASC	14	–	ns				Td MLCL – Tpl S257 SEL (max)
COL ADDR HOLD	TCAH	115	–	ns	CLKS, 6510			Td CLØ2L + THW
COL ADDR HOLD REF TO RAS	TAR	300	–	ns	CLKS, 6510			Td RLØH + THW
READ COMMAND SET UP	TRCS	130	–	ns	CLKS, 6510			TCHR – TMRWS
READ COMMAND HOLD	TRCH	30	–	ns	6510			TMRWH
WRITE COMMAND HOLD	TWCH	179	–	ns	CLKS, 6510			TCAS + TMRWH
WRITE COM HOLD REF TO RAS	TWCR	389	–	ns	CLKS, 6510			TRAS + TMRWH
WRITE COMMAND PULSE WIDTH	TWP	505	–	ns	CLKS, 6510			PWØHS – TMRWS + TMRWH
WRITE COM TO CAS LEAD	TCWL	475	–	ns	CLKS, 6510			PWØHS – TMRWS
DATA-IN SETUP TIME	TDS	80	–	ns	CLKS, 6510			TWCS – TMDS(DS); TCHW – TMXDS
DATA-IN HOLD TIME	TDH	135	–	ns	CLKS, 6510			Td CLØL + THW
DATA-IN HOLD REF TO RAS	TDHR	350	–	ns	CLKS, 6510			Td RLØL + THW
REFRESH PERIOD	TREF	–	>2	ms				
WRITE COM SETUP	TWCS	205	–	ns	CLKS, 6510			TCHW – TMRWS
CAS TO WE DELAY	TCWD	NA	–		NA			NA
RAS TO WE DELAY	TRWD	NA	–		NA			NA
RAS PRECHARGE TO CAS HOLD	TRPC	NA	–		NA			NA