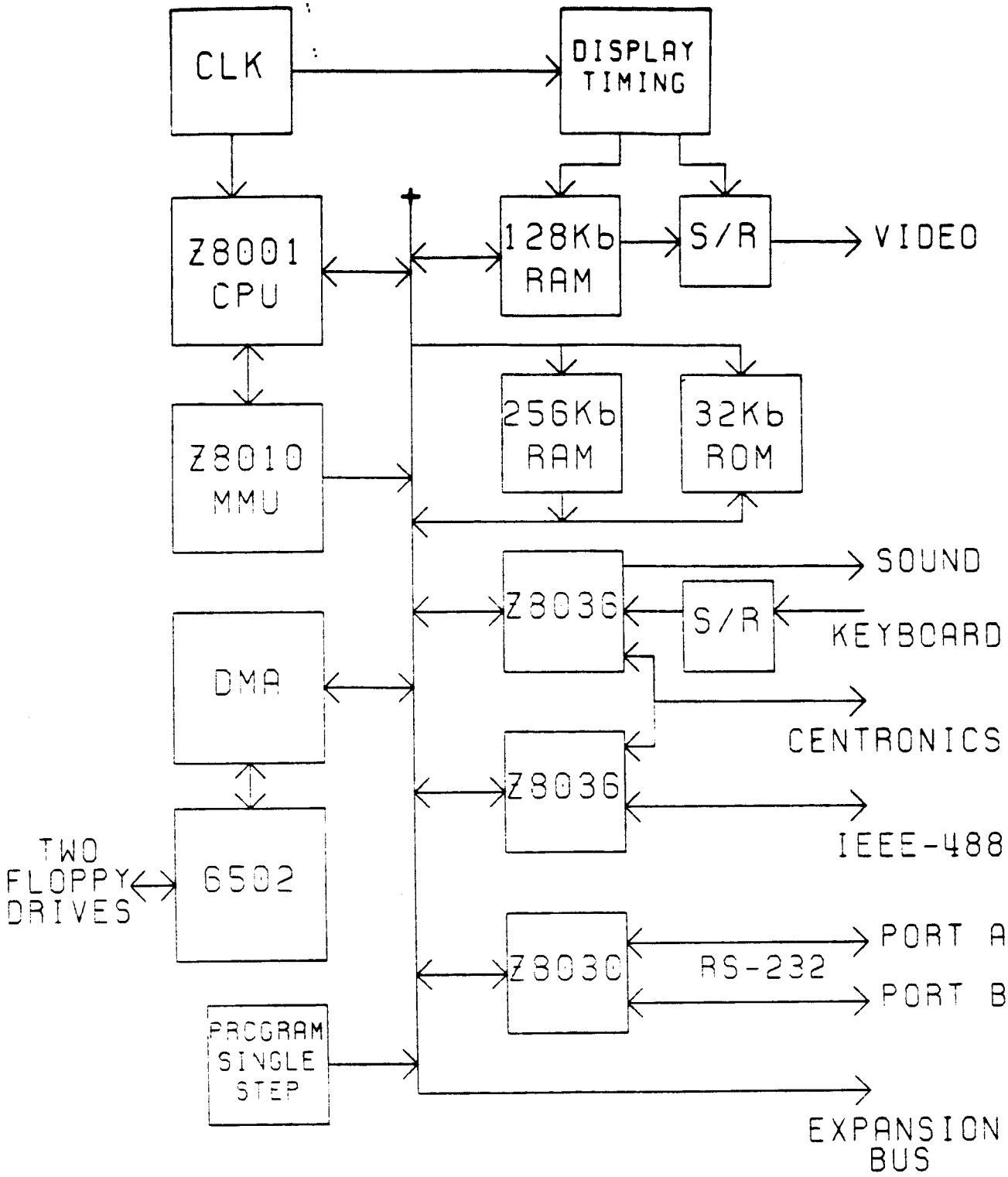


Z8000HR BLOCK DIAGRAM

COMMODORE		TITLE	Z8000HR HARDWARE SPECIFICATION
SIZE	DRAWING NO.	REV	SCALE / SHEET / OF

2.1 System Architecture

This section is designed to give a general description of system utilization and expandability. The following discussion refers to the block diagram on the previous page.

2.1.1 Overview

This computer is based on Zilog's Z8001 16 bit segmented CPU running at 6 MHz. All connections to this processor are made through Zilog's Z-Bus. One Z8010 MMU is used to translate the upper seven address lines and the seven segment number lines supplied by the CPU into 15 linear address lines. These lines, in conjunction with the lower nine untranslated address lines, are used to address all memory. ALL CPU memory transactions take place through the MMU. Normally the MMU uses the upper eight address line in the translation process. In order to reduce the hardware required for dynamic RAM support only seven are used in this system (i.e. A8 is not passed through the MMU). This reduction has the effect of altering the segment granularity from 256 to 512 bytes. Untranslated address lines are available strictly for use in the I/O space. All peripherals are addressed over the Z-Bus through this I/O space.

2.1.2 Memory Expansion

This unit can support up to 16M bytes combined total of ROM and RAM. The addition of ROM or RAM requires simply decoding some region of the linear address space and connecting it to the Z-BUS. However, this unit is not designed to supply power for any additional equipment. Therefore, the extra memory must be mounted exterally and must provide its own power. (See section on physical requirements)

2.1.3 Keyboard Interface

The keyboard for this unit is scanned using a single chip microprocessor (6500/1). This microprocessor, which resides in the keyboard and passes data serially to a snift register in the CPU box, is accessed through a Z8036 parallel I/O interface chip (See technical section for specific connections). This Z8036 is located at address 00-7F in the normal I/O space.

2.1.4 Display Interface

The display for this unit consists of a 1024 x 1024 pixel bitmapped screen. Each pixel corresponds to a bit in memory in segments 3E and 3F. The upper left most pixel is bit 15 (msb) of the word at 3E000000, the next pixel in that row is bit 14, etc. The lower right most pixel is bit 0 (lsb) of the word at 3F00FFFE. The timing for this display is generated by a 6845 located at address 400-4FF in the normal I/O space.

2.1.5 Sound Generation

Sound is produced by one of the counters in a Z8036 parallel I/O interface. This Z8036 is located address 80-FF in the normal I/O space.

2.1.6 Serial I/O

Serial I/O for this unit is achieved through a Z8030 serial communications controller (SCC). This device provides two channels which can be configured as RS-232 compatible ports. The SCC is located at address 100-1FF in the normal I/O space. The inputs and outputs of this chip are connected through standard RS-232 buffers to two DB-25S connectors, designated Port A and Port B.

2.1.7 IEEE-488 Interface

The IEEE interface is provided by a Z8036 parallel I/O interface which is conditioned by standard IEEE-488 line drivers and receivers. The Z8036 is located at address 80-FF in the normal I/O space.

2.1.8 Centronics Interface

The centronics interface uses the remaining lines on the keyboard and IEEE Z8036's. These lines are buffered by open collector TTL gates. The Z8036's are located at addresses 00-7F and 80-FF in the normal I/O space (See the technical section for specific pin connections).

2.1.9 Single Step

The ability to single step through programs is provided through the use of the non-vectored interrupt. This function is controlled by a latch at address 201 in the normal I/O space. When enabled, a NVI will be generated during every second instruction following the one which enabled it. If non-vectored interrupts are enabled, the interrupt will be processed at the end of the instruction during which the interrupt was generated.

2.1.10 Floppy Interface

The internal floppy disk drives are accessed through DMA. Commands are written in a predefined portion of the CPU's main memory, the floppy controller is interrupted by any I/O instruction using an address in the range 500-5FF, then the floppy controller takes over. For a more detailed description of the floppy interface refer to the floppy disk specification.

2.2 Software overview

All software supplied with the Z8000HR will run under the Coherent operating system. Coherent is a UNIX compatible, multi-tasking, multi-user operating system. The unit itself (ROM based software) will only contain diagnostics and boot code. Application languages such as BASIC and C will run under Coherent.

3.0 Technical Specification

This section provides the details for issues discussed in previous sections, as well as technical issues not yet mentioned.

3.1 Memory Configuration

The large memory space is controlled by a Zilog Z8010 MMU. All memory accesses pass through the MMU. A8 is always passed untranslated. This changes the segment granularity to 512 bytes instead of the usual 256 bytes. At power up, the MMU will pass addresses untranslated (MSEN bit of the mode register is set & TRANS bit is cleared). The control registers of the MMU are part of the Z8000's special I/O address space (address %00FC).

The physical memory map of the Z8000M computer is shown below. The map is shown by segment number.

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	ROM	-	RAM	RAM	RAM	RAM	-	-	-	-	-	-	-	-	-	-
1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	DSP	DSP
4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

This memory map clearly shows how much room there is for memory expansion (a "-" shows possible expansion area).

DSP - Display RAM.

3.2.1 Keyboard

The keyboard for this device must support the full ASCII character set (i.e. must have all alphanumeric characters and a control key). The keyboard can be broken up into five groups of keys; alphanumeric, keypad, cursor control, function and special function. These groups contain the following keys:

Alphanumeric

26	A-Z
10	0-9
1	Space
11	Symbols
3	Shift keys (2 shift, 1 lock)
2	Control (cntrl, alt)
1	Return
1	Tab
1	Escape
1	Backspace
1	Delete

Keypad

10	0-9
1	Decimal point
1	00
1	Enter
5	Symbols (?+-*/)
1	CE

Cursor control

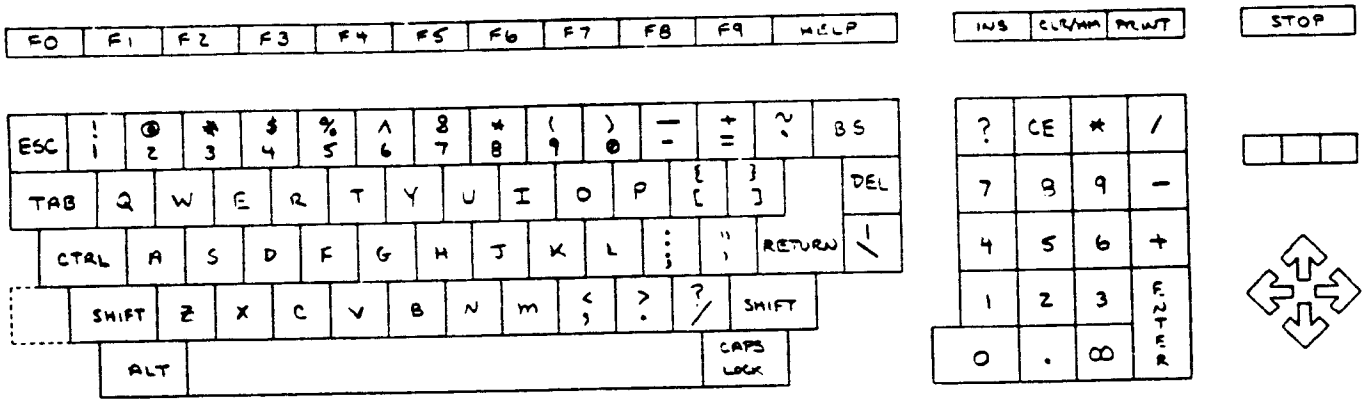
4	Direction keys

Function

10	F0-F9
3	Mouse function keys

Special function

1	Help
1	Stop
1	Insert
1	Home/Clr
1	Screen print



Proposed keyboard layout

COMMODORE		TITLE	Z8000HR HARDWARE SPECIFICATION
SIZE	DRAWING NO.	REV	
		SCALE	SHEET OF

3.2.2 Keyboard Interface

Keyboard scanning is done by a 6500/1 single chip microprocessor which resides in the keyboard unit. This device contains four 8-bit parallel ports. Of the 32 I/O lines available, 22 (PA0-PA7, PB0-PB7, PC0-PC5) are used to scan the keyboard, 4 are general purpose configuration lines (PD0-3) and 4 (PD4-PD7) are used to communicate with the Z8000 through a shift register and Z8036. PD7 supplies data to the shift register which is clocked in by PD6. Once the eight bits of the character from the keyboard have been clocked into the shift register the handshake lines are used to transfer the data from the shift register to the Z8036. PC6 is an input to the Z8036 and is used to indicate the availability of data. PC7 is an ouput from the Z8036 and indicates that the data has been accepted. This corresponds to the interlocked handshake mode of the Z8036. There are a total of six lines which connect the keyboard to the CPU, these include: +5V, GND, DATA, CLK, DAV, RFD.

Z8036 (%0000-007F)

Port A	: PA0	PA1	PA2	PA3	PA4	PA5	PA6	PA7
6500/1 data	: KD0	KD1	KD2	KD3	KD4	KD5	KD6	KD7

Port C	: PC0	PC1	PC2	PC3
Kbd handshake	: CBSY	60Hz	PD4	PD5

KD0-KD7 are keyboard data lines from shift register.
PD4 and PD5 are 6500/1 lines
CBSY is a centronics line

3.3 Display

The display for this unit consists of a 1024 x 1024 pixel bitmapped screen. Each pixel corresponds to a bit in memory in segments 3E and 3F. (Bit = 1 = illuminated) The upper left most pixel is bit 15 (msb) of the word at 3E000000, the next pixel in that row is bit 14, etc. The lower right most pixel is bit 0 (lsb) of the word at 3F00FFFE. The timing for this display is generated by a 6545 located at address 400-4FF in the normal I/O space. (401 - address register, 403 - data register).

The character clock for the 6545 is 3MHz which is the basis for the horizontal and vertical times. Currently the monitor is being scanned at a horizontal frequency of 32kHz and a vertical rate of 60Hz interlaced. These frequencies are completely programmable and it may become necessary to adjust them for flicker free performance.

3.4 Sound Generation

Sound is generated by counter/timer #2 of the Z8036 at address 80-FF. This Z8036 is clocked at 750kHz giving a minimum frequency of about 5Hz. Counter #2 should be programmed to provide an external output (PB0). To generate more complex sounds it can be internally linked to counter/timer #1. This counter can be used to give a tone of a certain duration or used to modulate the output with another square wave. The diagram below illustrates the particular bit connections.

Z8036 (%0080-00FF)

Port B :	PB0	PB1	PB2	PB3	PB4	PB5	PB6	PB7
	SND	#	#	#	#	#	#	#

SND - Sound output
\# - IEEE control

3.5 RS-232 Interface

Two RS-232 ports are provided through the use of the Z8030 SCC (Serial Communications Controller). This is located in the normal I/O space at address 100-1FF. This chip must be programmed to use the asynchronous RS-232 compatible protocol. The receive and transmit clocks provided to the Z8030 are 6MHz, the following table gives the values which must be programmed into the chip to provide the standard RS-232 baud rates.

Z8030A with 6MHz clock (x16 clock mode in all cases)

Desired baud rate	Time constant (hex)	Actual baud rate
50	0EA4	50.0
75	09C3	75.0
110	09A8	110.0
134.5	0971	134.5
150	04E1	150.0
300	026F	300.3
600	0137	599.6
1200	009A	1203.0
1800	0066	1804.6
2000	005C	1996.5
2400	004C	2406.1
3600	0032	3609.1
4800	0025	4809.0
7200	0018	7218.2
9600	0012	9383.0
19200	0008	19248.0

3.6 Centronics Interface

A centronics parallel port is provided by buffering a Z8036 port with open collector TTL drivers. Eight data lines and three control lines are supported. They are distributed over two Z8036's as follows:

Z8036 (%0000-007F)

Port B	PB0	PB1	PB2	PB3	PB4	PB5	PB6	PB7
Centronics Data:	CD0	CD1	CD2	CD3	CD4	CD5	CD6	CD7

Port C	PC0	PC1	PC2	PC3
Cent. Control :	CBSY	60Hz	*	*

Z8036 (%0080-00FF)

Port B	PB0	PB1	PB2	PB3	PB4	PB5	PB6	PB7
Cent. Control :	$	ACK	#	#	#	#	#	#

Port C	PC0	PC1	PC2	PC3
Cent. Control :	#	#	#	CDS

* - Keyboard control
\# - IEEE-488 control
$ - Sound output

3.7 IEEE-488 Interface

The IEEE-488 interface is provided in the form of buffered port lines of a Z8036. The conditioning is done by 75160 and 75161 line drivers and receivers. The table below shows the connections to the ports of the Z8036.

Z8036 (%0080-00FF)

Port A	PA0	PA1	PA2	PA3	PA4	PA5	PA6	PA7
IEEE-488 data	D1	D2	D3	D4	D5	D6	D7	D8
Port B	**PB0**	**PB1**	**PB2**	**PB3**	**PB4**	**PB5**	**PB6**	**PB7**
IEEE Control	$	*	SRQ	ATN	DAV	EOI	NDAC	NRFD
Port C	**PC0**	**PC1**	**PC2**	**PC3**				
IEEE Control	IFC	TE	DC	*				

The remote enable signal, REN, is controlled by bit 0 of a latch at 203 in the normal I/O space. This latch is set to zero on powerup.

* - Centronics control lines
$ - Sound output
DC,TE - Control lines for 75160 and 75161

3.8 Single Step Control

The control of the single stepper is accomplished through bit 0 of a latch located at address 201 in the normal I/O space. On powerup this line is set low. Bit 0 must be set in order to enable the single stepper logic. The NVI line to the Z8000 will be asserted during the second instruction following the one which sets bit 0 and will be reasserted on every second instruction until the bit is once again cleared. The Z8000 will enter the NVI processing routine at the completion of the instruction during which NVI was asserted if NVI interrupts are enabled.

3.9 Floppy Disk Interface

The internal floppy disk drives are accessed through DMA. Commands are written into a predefined portion of the CPU's main memory, the floppy controller begins to process the command when interrupted by any I/O instruction using an address in the range 500-5FF, then the floppy controller takes over. For a more detailed description of the floppy disk interface see the floppy disk specification.

3.10 I/O Map

The following table lists the used and reserved addresses in the normal I/O space.

0000-007F	Z8036 - Keyboard/TOD/Centronics
0080-00FF	Z8036 - IEEE-488/Centronics/Sound
0100-01FF	Z8030 - Serial I/O
0200-02FF	System latches
0300-03FF	Color display
0400-04FF	Bitmap display
0500-05FF	Floppy disk controller
0600-06FF	Winchester disk controller
0700-07FF	** UNUSED **
0800-FFFF	** UNUSED **

3.11 Vectored Interrupt Priority

In accordance with the Z-Bus, vectored interrupts are prioritized using a daisy chain. Both ends of the chain are supplied to the expansion connector to allow peripherals to have either the highest or the lowest priority in the chain. On the CPU board the peripherals are prioritized in the following order.

1. APU when installed. (Highest)
2. Keyboard - Z8036, also used for time of day.
3. RS-232 - Z8030.
4. IEEE - Z8036.
5. Floppy disk controller. (Lowest)

3.12 Arithmetic Co-processor

A 60 pin dual in-line header will be provided on the circuit board to connect to an added circuit board which will contain the Z8070 arithmetic coprocessor.

3.13 Power Supply

The power supply for this unit will be of the switching type. The following table shows the maximum current requirements for the individual voltages.

+5V @8.00A
+12V @2.50A
-12V @0.05A

NOTE: CBM II HP PWR SUPPLY
+5 @ 5.5A
+12 @ 2.5A
+12 #2 @ 1.5A
-12 @ 0.3A
~~9V AC FOR 60 HZ/50 HZ TOD SIGNAL~~
LINE FREQ TTL O.C OUTPUT

3.14 Estimated Cost

The estimated cost of this unit is $633. The table below breaks down this price by functional units.

Case	45.00
Monitor	150.00
Keyboard	20.00
PC Board	25.00
Floppy Drive	130.00
CPU Components	137.50
Display	64.65
Floppy Cont.	28.95
Power Supply	32.00
	$633.10

4.0 Packaging Considerations

This section provides the requirements for housing the Z8000HR computer and its associated peripherals.

4.1 Internal Space Requirements

4.1.1 Display

This unit will contain a 15" high resolution black and white picture tube and associated driving electronics. A five pin connector must be provided on the monitor and the CPU enclosures for interconnection.

4.1.2 Board Area

The PC board, before cost reduction, contains about 165 integrated circuits, requiring approximately 280 square inches.
THE FINAL PCB SIZE _____?

4.1.3 Power Supply

The maximum dimensions of the power supply are 4.25 x 3.75 x 1.75 inches and will be mounted in the CPU box. POWER DISSIPATION ?

4.1.4 Floppy Drive

Space must be provided in the CPU box for two 5 1/4" floppy drives. NATIONAL JU-570-2 OR EQUIVALENT. POWER DISSIPATION ?

4.2 Switches

Only two switches are required in addition to the keyboard. These are a power switch and a reset button. Both preferably mounted on the rear panel. PWR SWITCH IS NOT PART OF SUPPLY ?

4.3 External Connections

The following connectors must be mounted on the rear panel of the unit:

1. One video connector
2. Two RS-232 connectors
3. One IEEE-488 connector
4. One centronics connector
5. One 120VAC line connector
6. Three expansion connectors

ACCESS SLOT REQ.

A keyboard and a mouse connector must be provided elsewhere on the CPU enclosure.

4.4 Expansion

Expansion of this unit will be accomplished by extending the Z-BUS into another box. This box will be equiped with its own power supply and provide slots into which future peripherals and add-ons will fit. This box will be connected to the main unit by three 64 conductor ribbon cables. It is important that these cables be as short as possible. Therefore, these two enclosures should be designed to be positioned as close as possible without obstructing access to other connectors or switches. Provisions should also be made to allow a heavy ground strap between the two units.